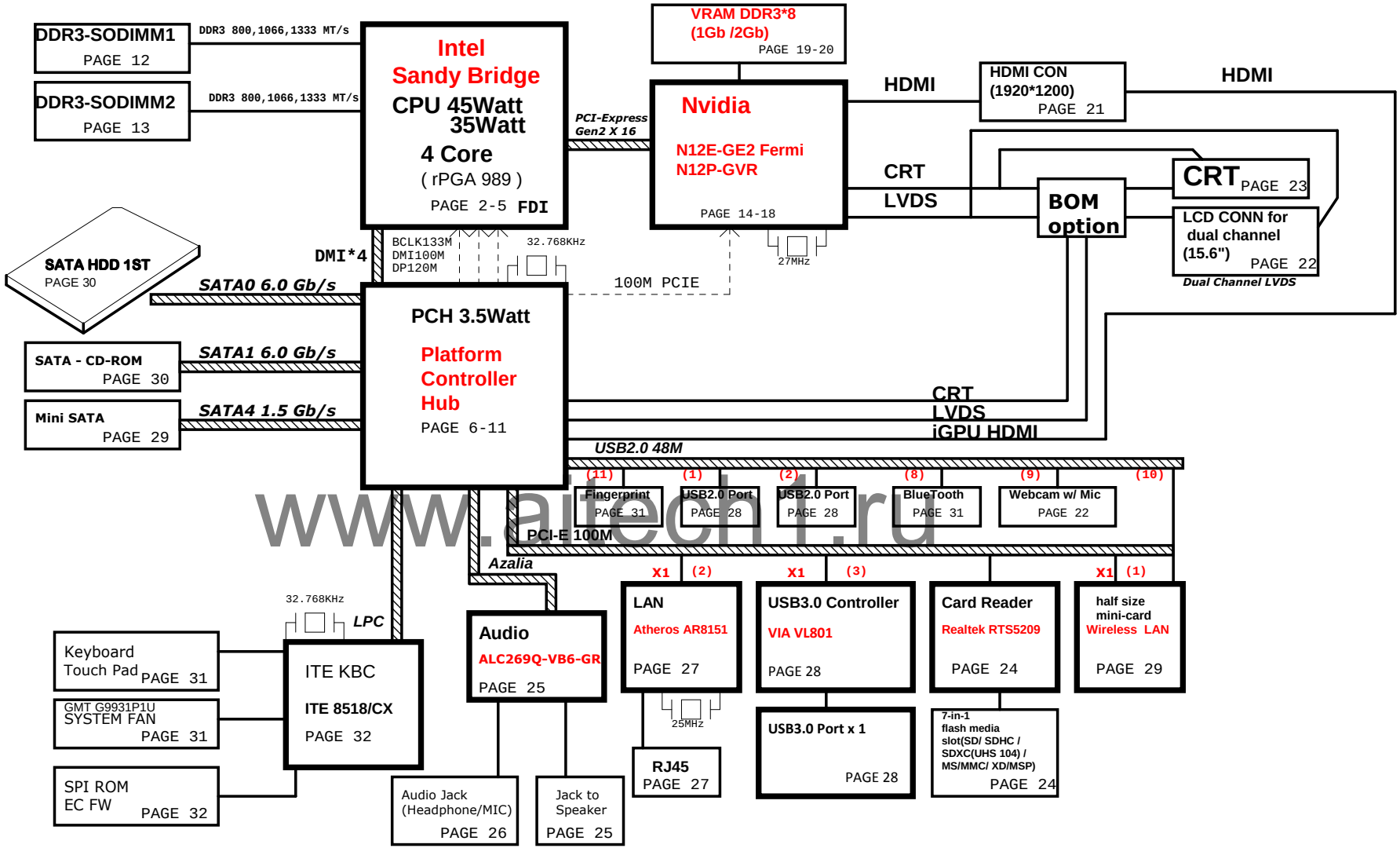
LG Raffaello2 QLM 15.6" BLOCK DIAGRAM

01

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT



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DDR III SMDDR_VTERM and GPU+1.5V/+1.0V(RT8207G) PAGE 40

BATTERY SELECTOR PAGE 42

SYSTEM CHARGER(P2806) PAGE 41

SYSTEM POWER RT8206B PAGE 35

+1.05V_VTT and GPU +1.8V/+3V(VT358) PAGE 38

VCCP +1.05V/+1.8V(RT8204) PAGE 36

VGACORE/VDDCI(RT8208/RT9018A) PAGE 39

CPU CORE (ADP3212) PAGE 37

NB5

PROJECT : QLM
Quanta Computer Inc.

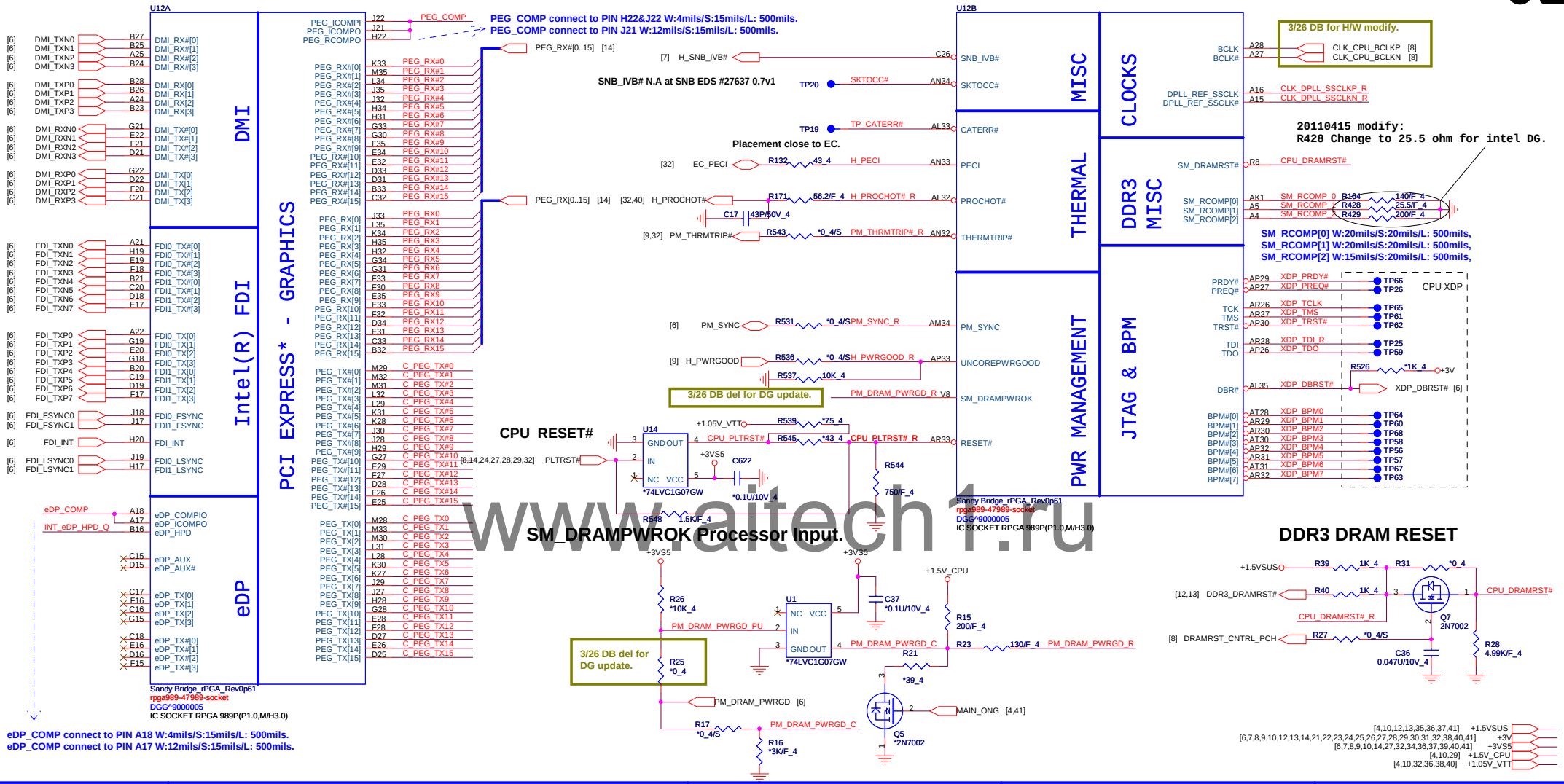
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Friday, May 20, 2011 Sheet 1 of 42

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02



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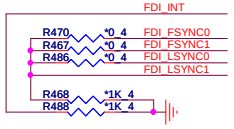
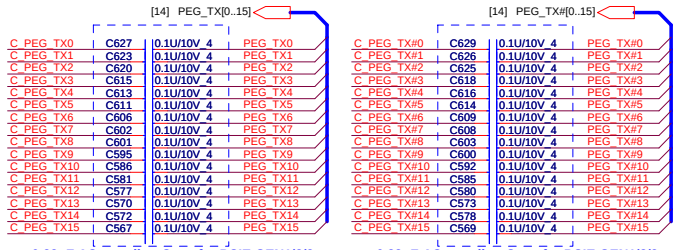
FDI disable (DIS only stuff)

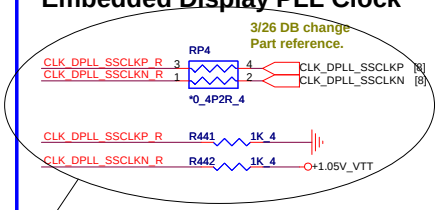


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

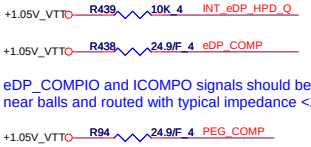


Embedded Display PLL Clock



20110418 modify:
1. RP4 change to unstuff for no ePD.
2. CLK_DPLL_SSCLKP_R change to pull down 1K.
3. CLK_DPLL_SSCLKN_R change to pull up 1K.

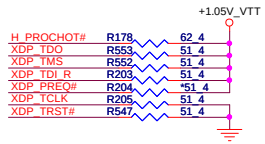
DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



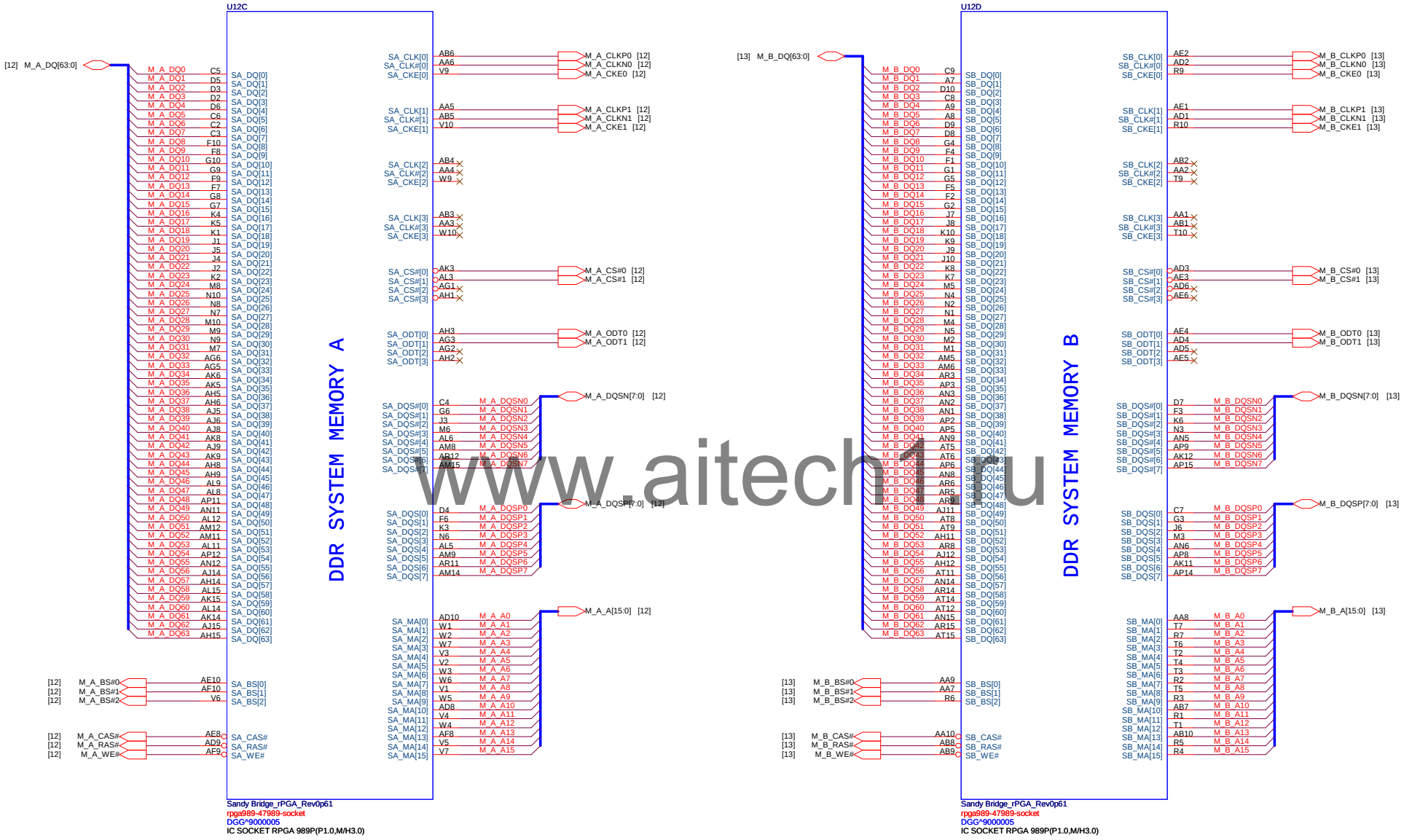
H_PROCHOT#	R178	62_4
XDP_TDO	R553	51_4
XDP_TMS	R552	51_4
XDP_TDI_R	R203	51_4
XDP_PREQ#	R204	*51_4
XDP_TCLK	R205	51_4
XDP_TRST#	R547	51_4

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A
Date: Friday, May 20, 2011	Sheet 2 of 42	

Sandy Bridge Processor (DDR3)



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NB5

PROJECT : QLM
Quanta Computer Inc.

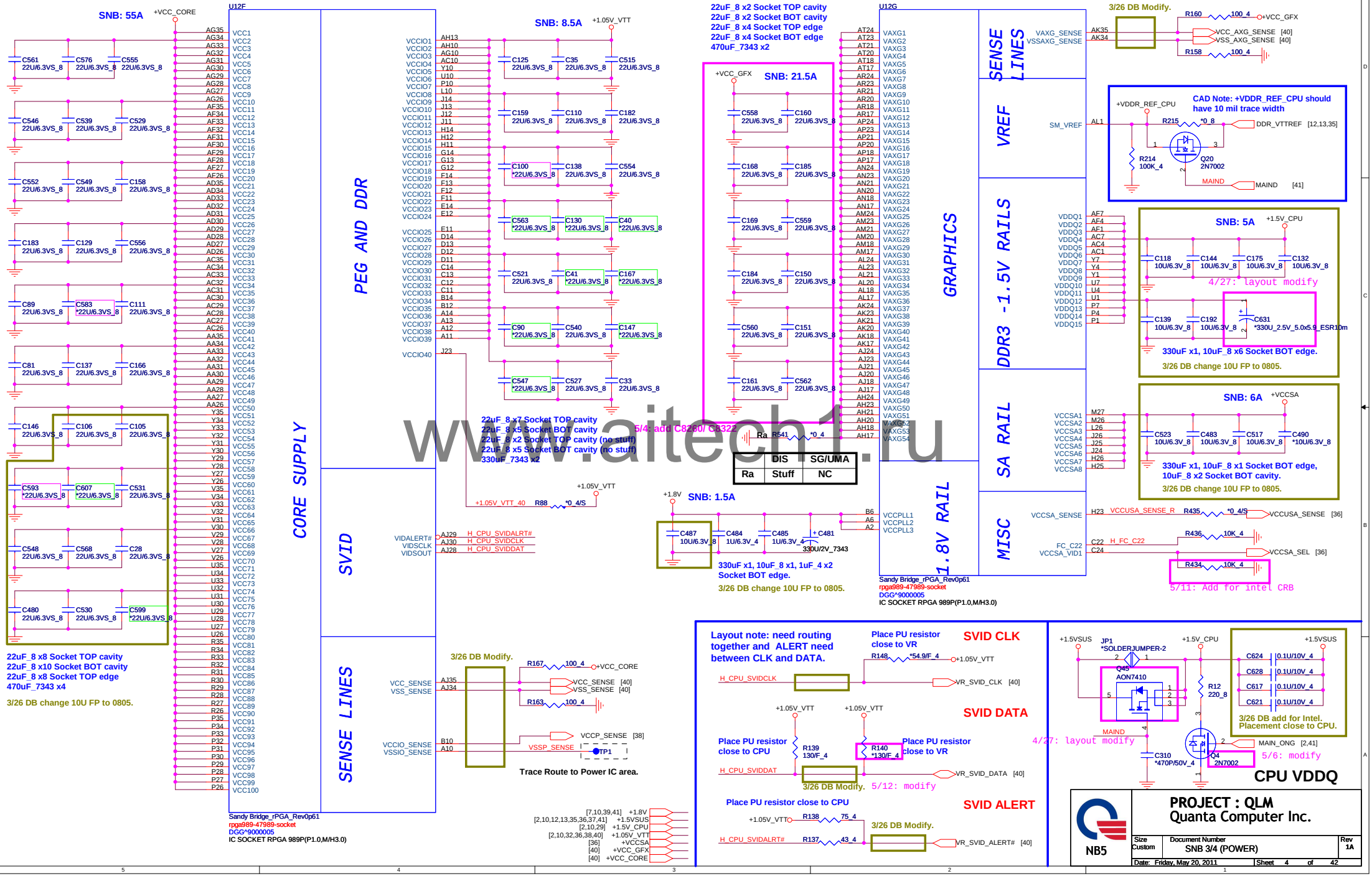
Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

Date: Friday, May 20, 2011 | Sheet 3 of 42

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04



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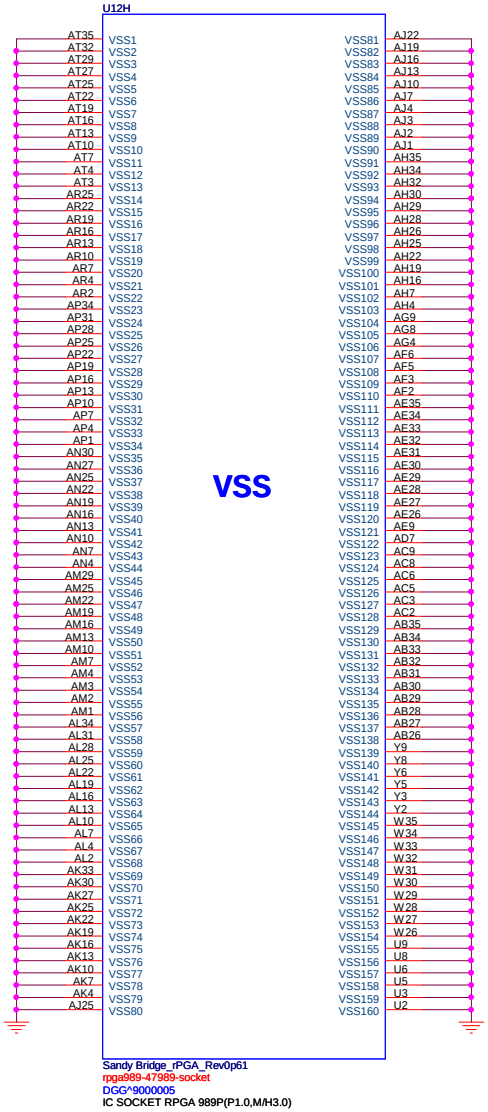
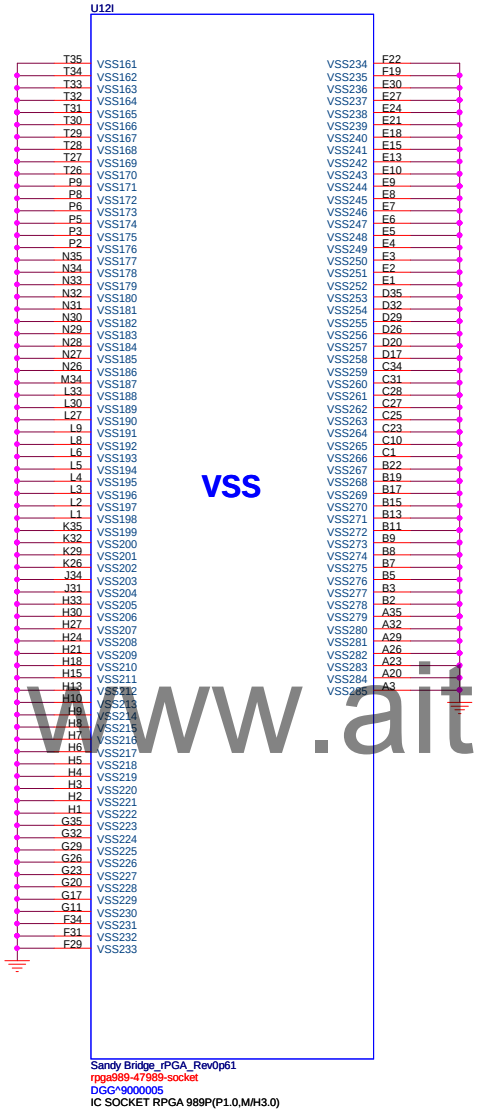
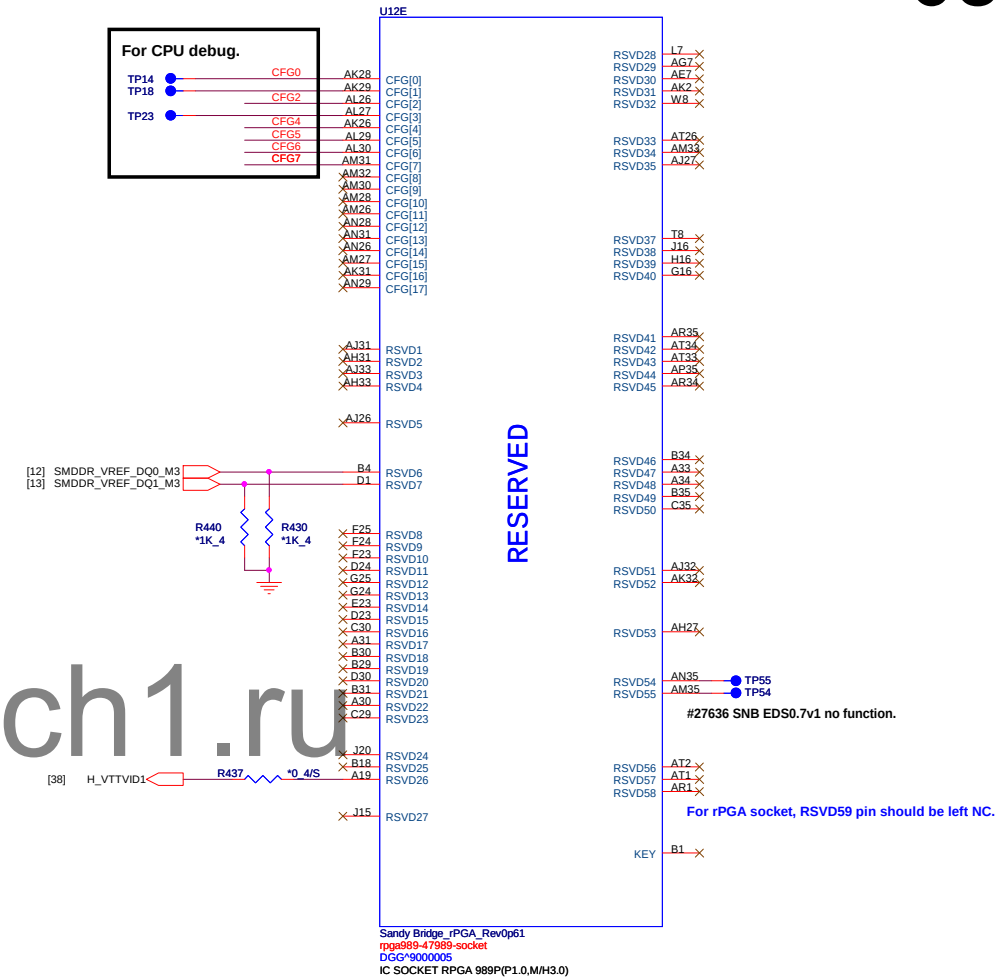
Sandy Bridge Processor (GND)





Sandy Bridge Processor (RESERVED, CFG)



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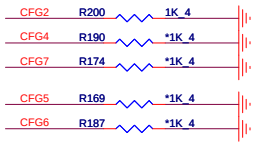
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

NB5

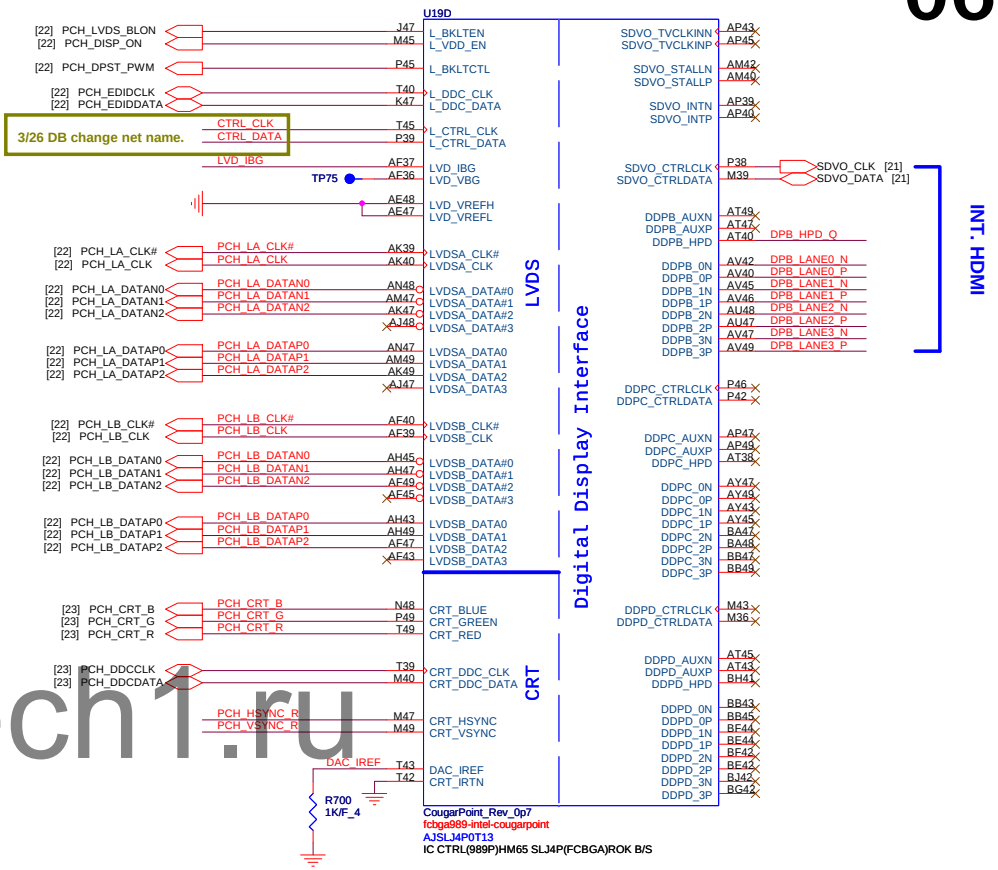
PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Friday, May 20, 2011 Sheet 5 of 42

Cougar Point (DMI,FDI,PM)

Cougar Point (LVDS,DDI)



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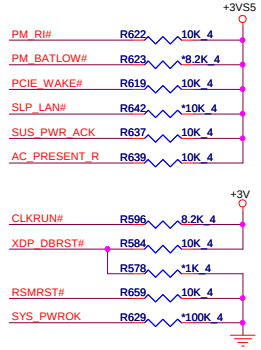
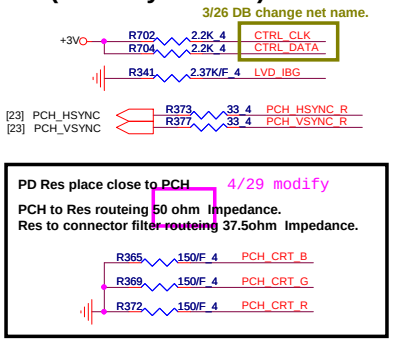
[7,10,21,22,23,25,26,29,30,31,41] +5V
[2,7,8,9,10,12,13,14,21,22,23,24,25,26,27,28,29,30,31,32,38,40,41] +3V
[2,7,8,9,10,14,27,32,34,36,37,39,40,41] +3VS5
[7,22,31,32,33,34,41] +3VPCU
[7,10] +3V_DSW
[7,10,32] +3V_RTC
[7,8,10,28,37,39] +1.05V

PCH Pull-high/low(CLG)

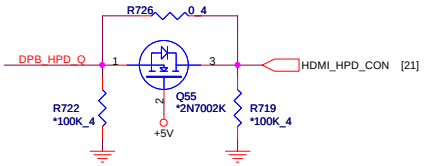


INT LVDS & CRT disable (DIS only remove)

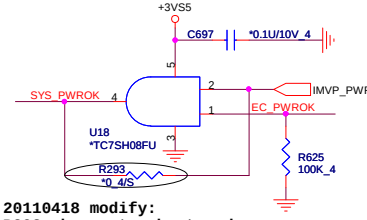


INT HDMI disable (DIS only remove)

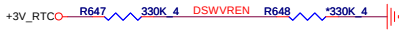
INT HDMI Detect Function



System PWR_OK(CLG)

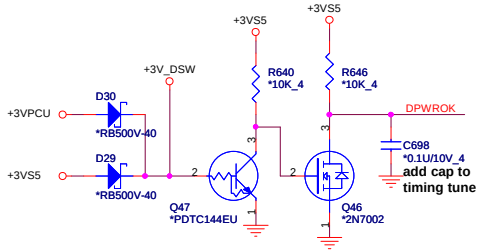


20110418 modify:
R293 change to short pad.



On Die DSW VR Enable
High = Enable (Default) Low = Disable

DPWROK FOR DSW



NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
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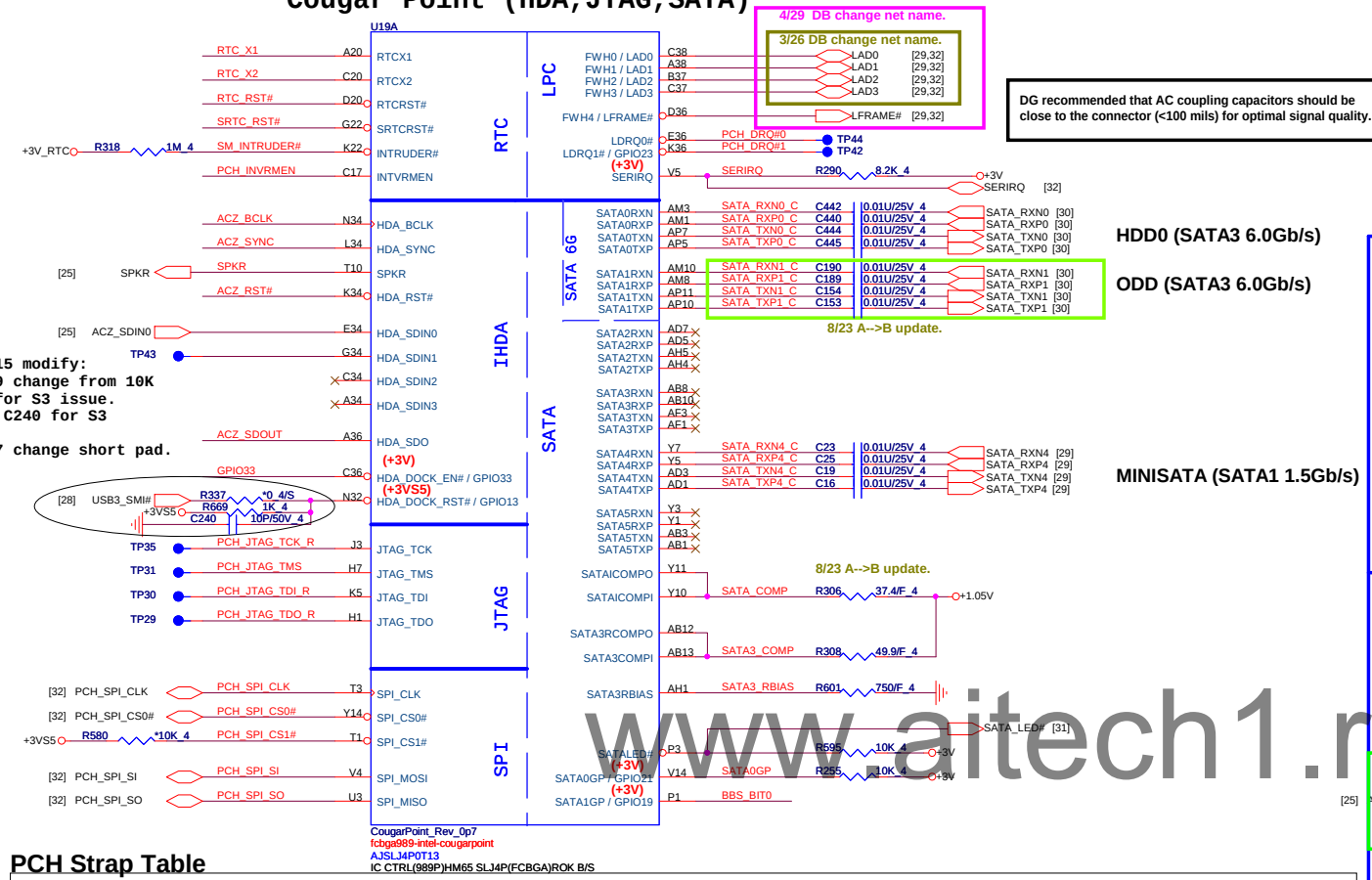
06

Cougar Point (HDA,JTAG,SATA)



4/29 DB change net name.

3/26 DB change net name.

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

HDD0 (SATA3 6.0Gb/s)

ODD (SATA3 6.0Gb/s)

8/23 A-->B update.

MINISATA (SATA1 1.5Gb/s)

8/23 A-->B update.

20110415 modify:
1. R669 change from 10K to 1K for S3 issue.
2. Add C240 for S3 issue.
3. R337 change short pad.

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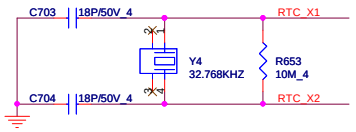
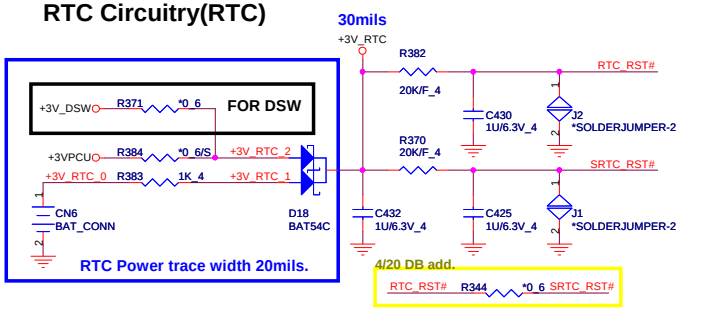
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R571 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R698 *1K_4, R713 10K_4, +3V, PCI_GNT3# [8], Bios request, for can't boot Capella 4/28
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R650 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R672 *1K_4 GPIO33_E [32] 8/23 A-->B update.
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → Boot Location SPI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# 1, GNT0# 0 → Boot Location LPC	R577 *1K_4, R703 *1K_4, BBS_BIT0, BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R602 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 reserve.	+1.8V R603 2.2K_4, R615 4.7K_4, NV_CLE [8], H_SNB_IVB# [2] N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R356 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[3] GPIO33_E, ACZ_SDOUT, R674 *1K_4 +V3.3A_1.5A_HDA_IO 8/23 A-->B update.
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R627 *1K_4 ICC_EN# [9] 4/29 reserve.
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R609 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R632 1K_4 +3V

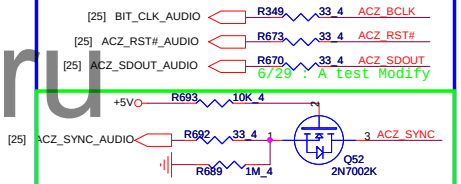
RTC Clock 32.768KHz



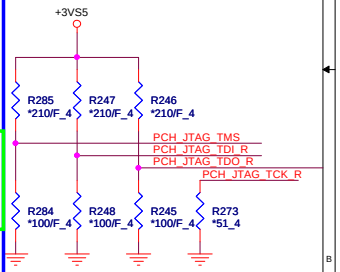
RTC Circuitry(RTC)



HDA Bus(CLG)

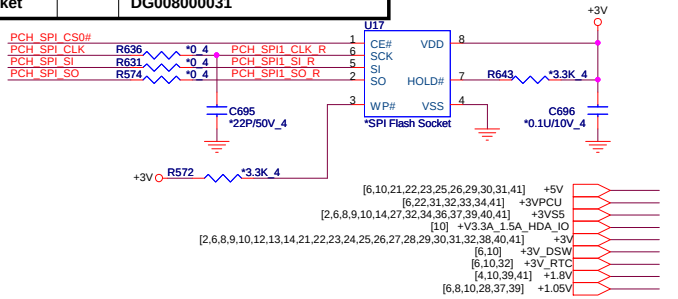


PCH JTAG Debug(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH SPI ROM(CLG)



NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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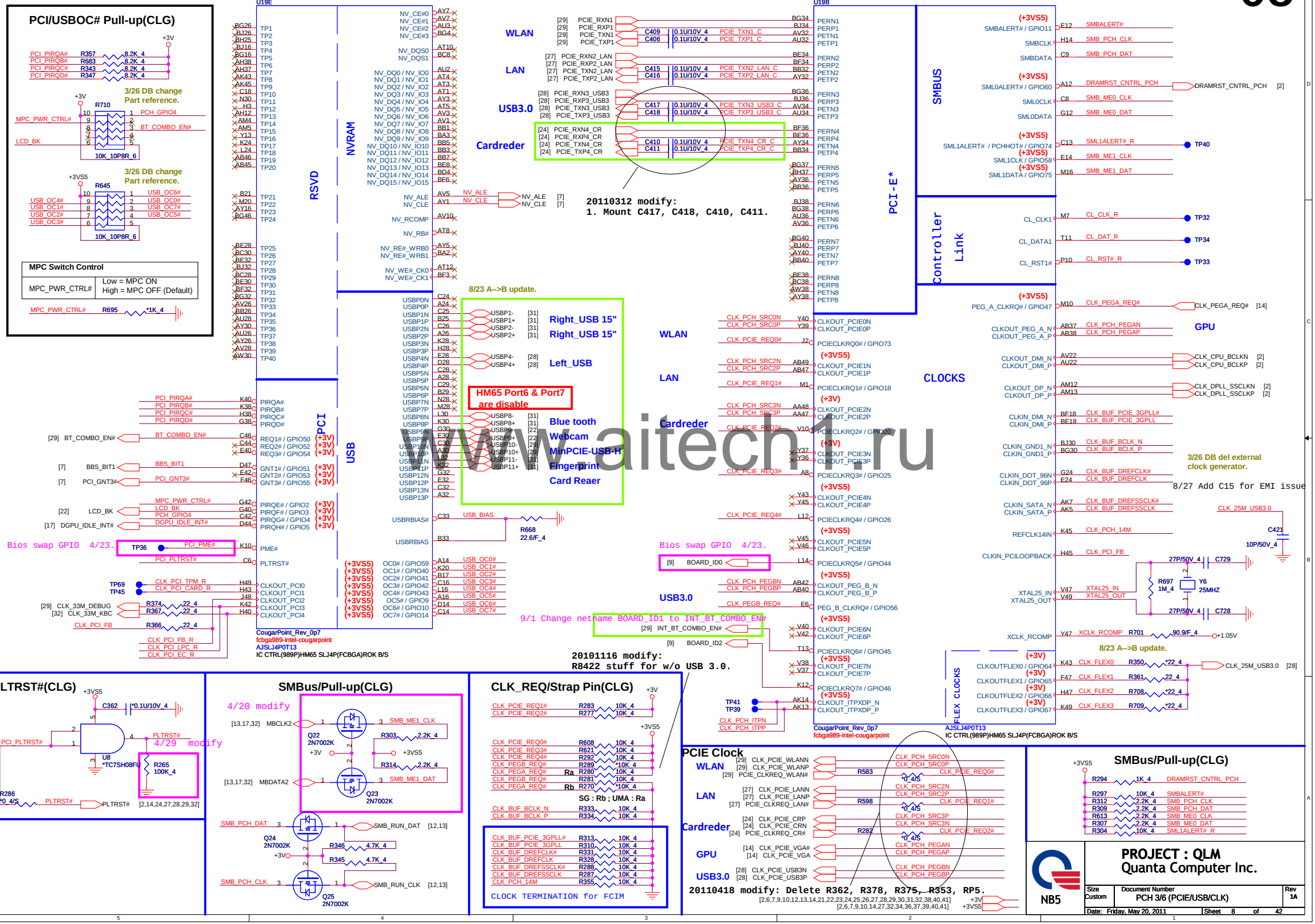
07

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08



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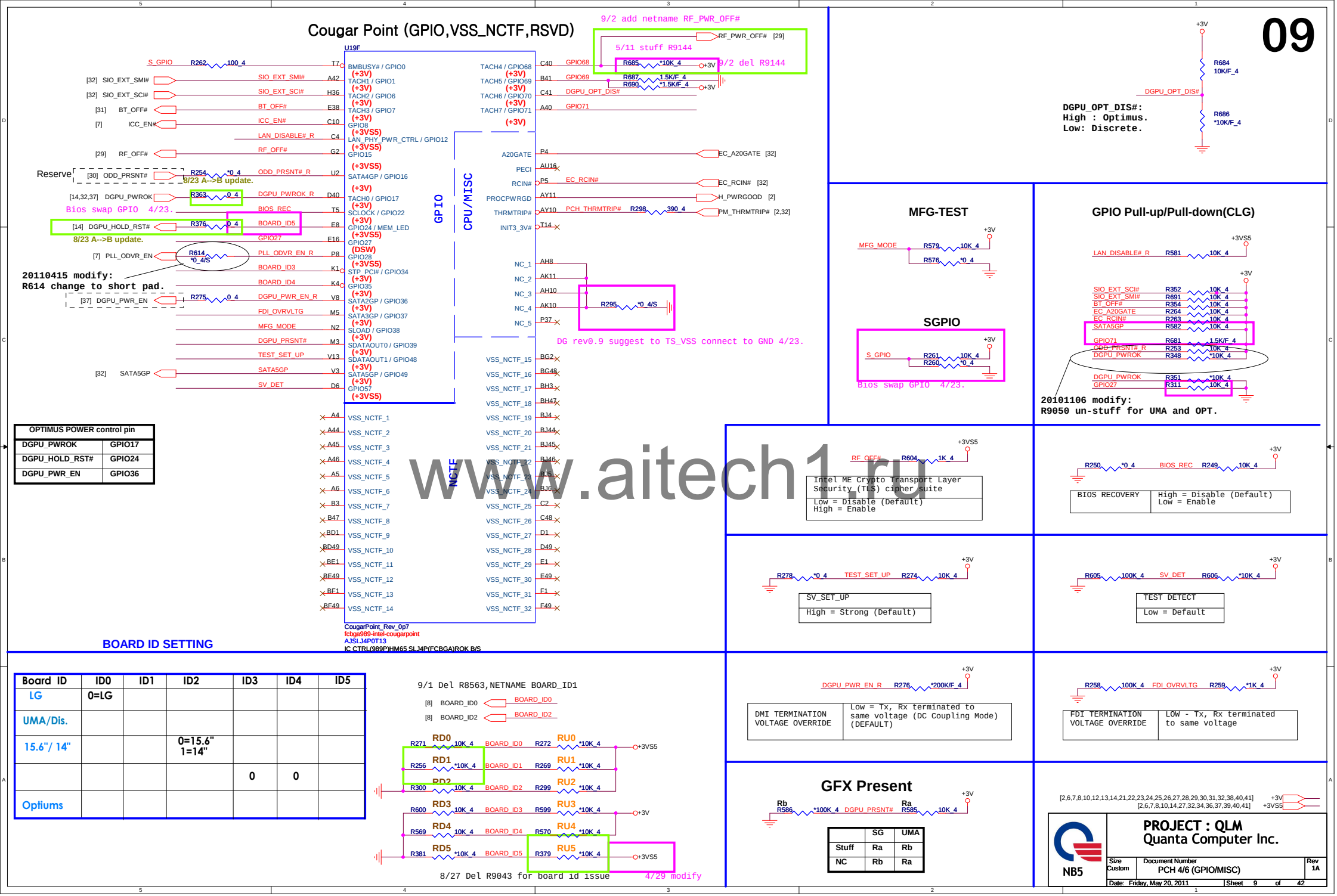
Cougar Point (GPIO,VSS_NCTF,RSVD)



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LG	0=LG					
UMA/Dis.						
15.6"/ 14"			0=15.6" 1=14"			
				0	0	
Optiums						

9/1 Del R8563,NETNAME BOARD_ID1

8/27 Del R9043 for board id issue 4/29 modify

DGPU_OPT_DIS#:
High : Optimus.
Low: Discrete.

MFG-TEST

SGPIO

Bios swap GPIO 4/23.

GPIO Pull-up/Pull-down(CLG)

20101106 modify:
R9050 un-stuff for UMA and OPT.

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

[2,6,7,8,10,12,13,14,21,22,23,24,25,26,27,28,29,30,31,32,38,40,41] +3V
[2,6,7,8,10,14,27,32,34,36,37,39,40,41] +3VS5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
Date: Friday, May 20, 2011	Sheet 9 of 42	

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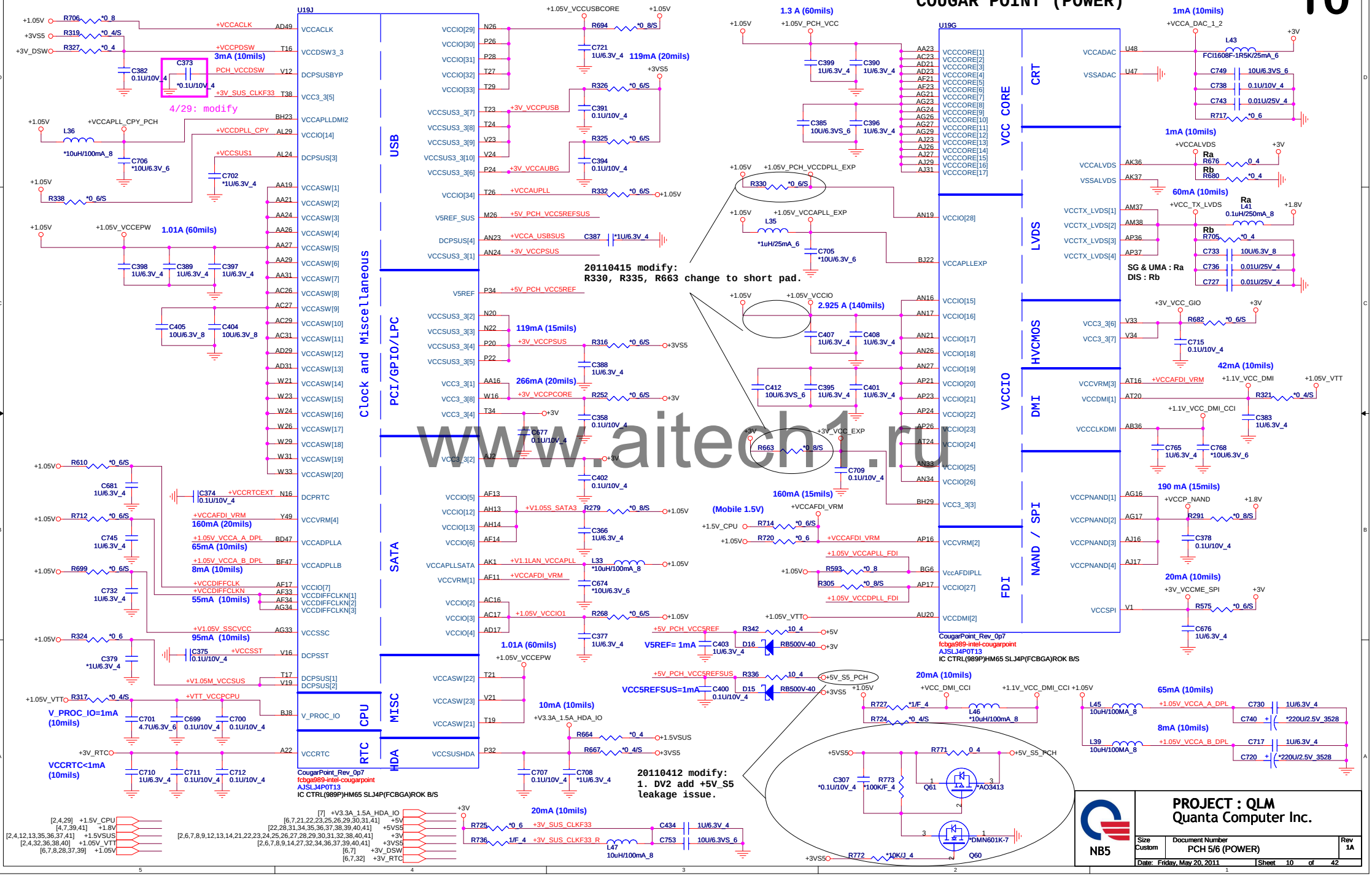
Cougar Point-M (POWER)

COUGAR POINT (POWER)

10



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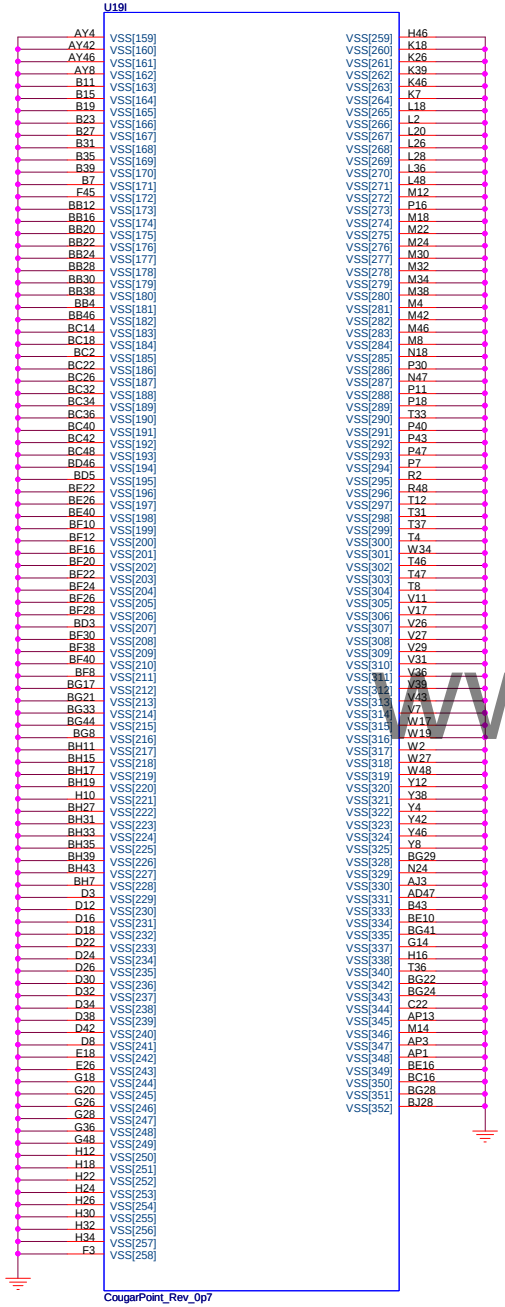
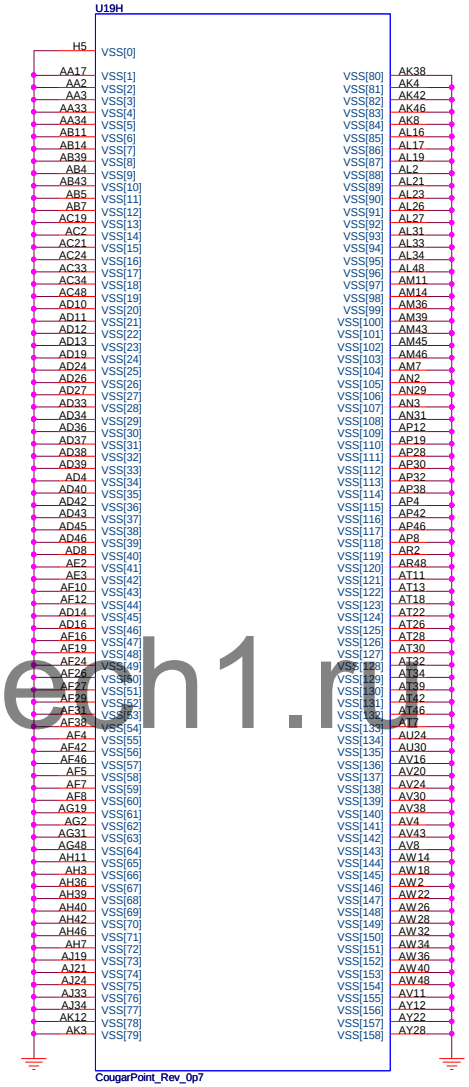
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)



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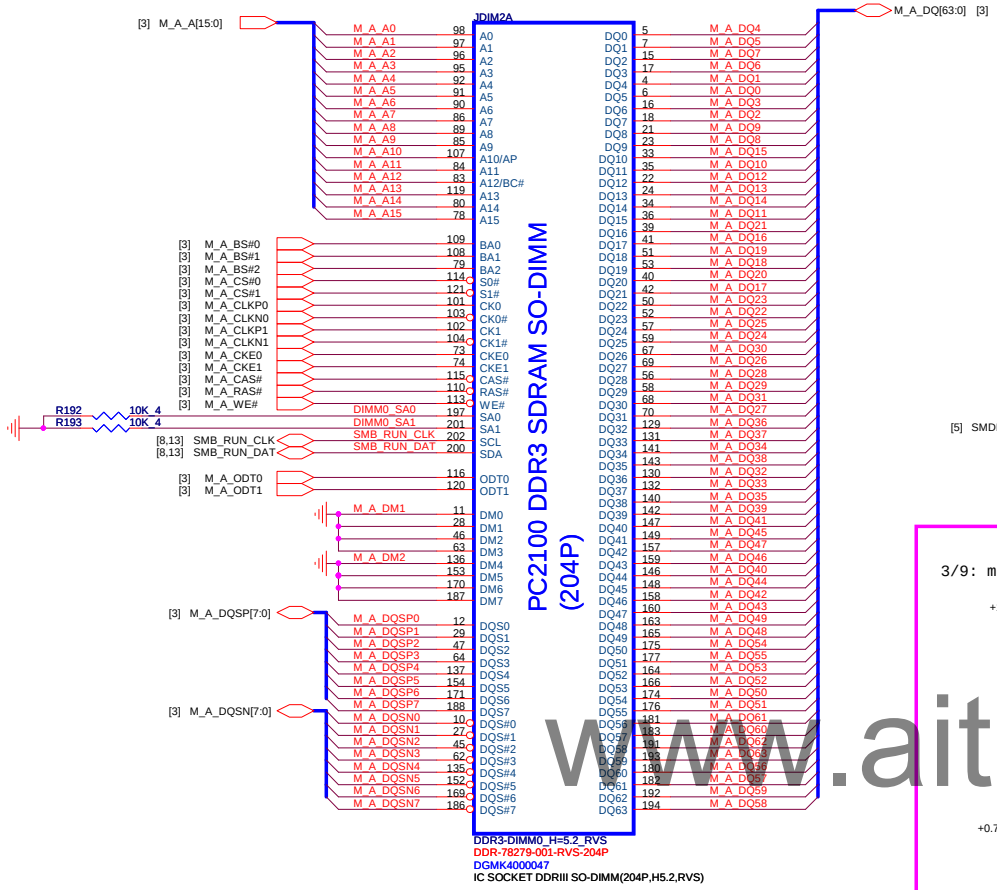
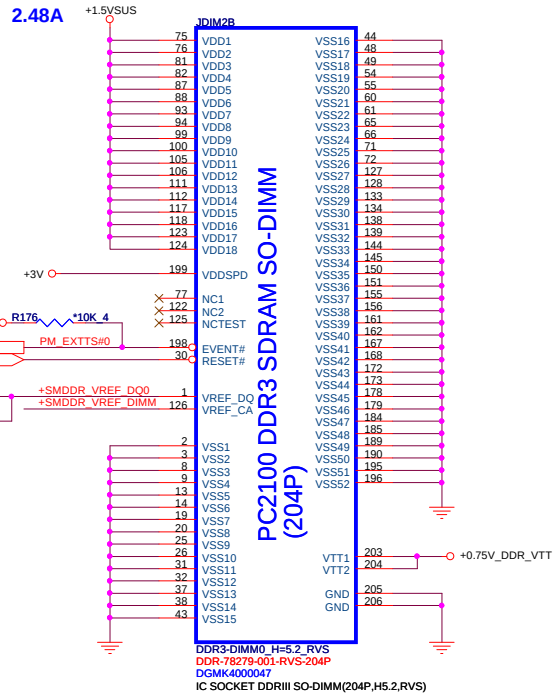
NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

Date: Friday, May 20, 2011 Sheet 11 of 42





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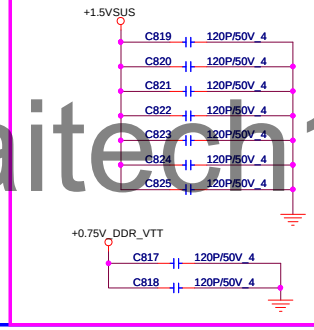
3/9: modify EMI Solution

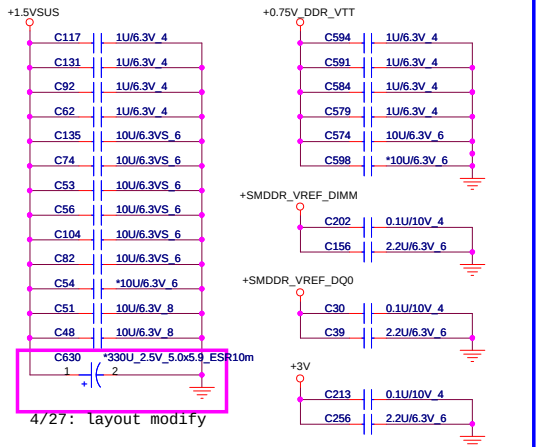


VREF DQ0 M2 Solution

6/29: Del M2 solution

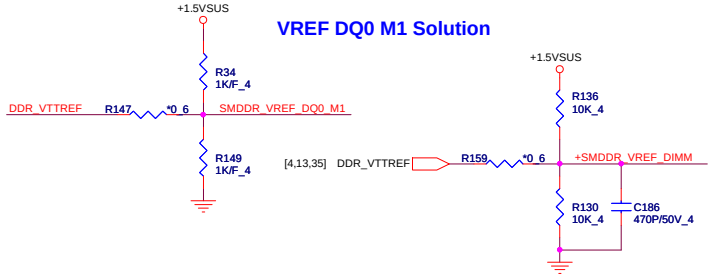
4/29: reserve M2 solution

Place these Caps near So-Dimm0.



4/27: layout modify

VREF DQ0 M1 Solution



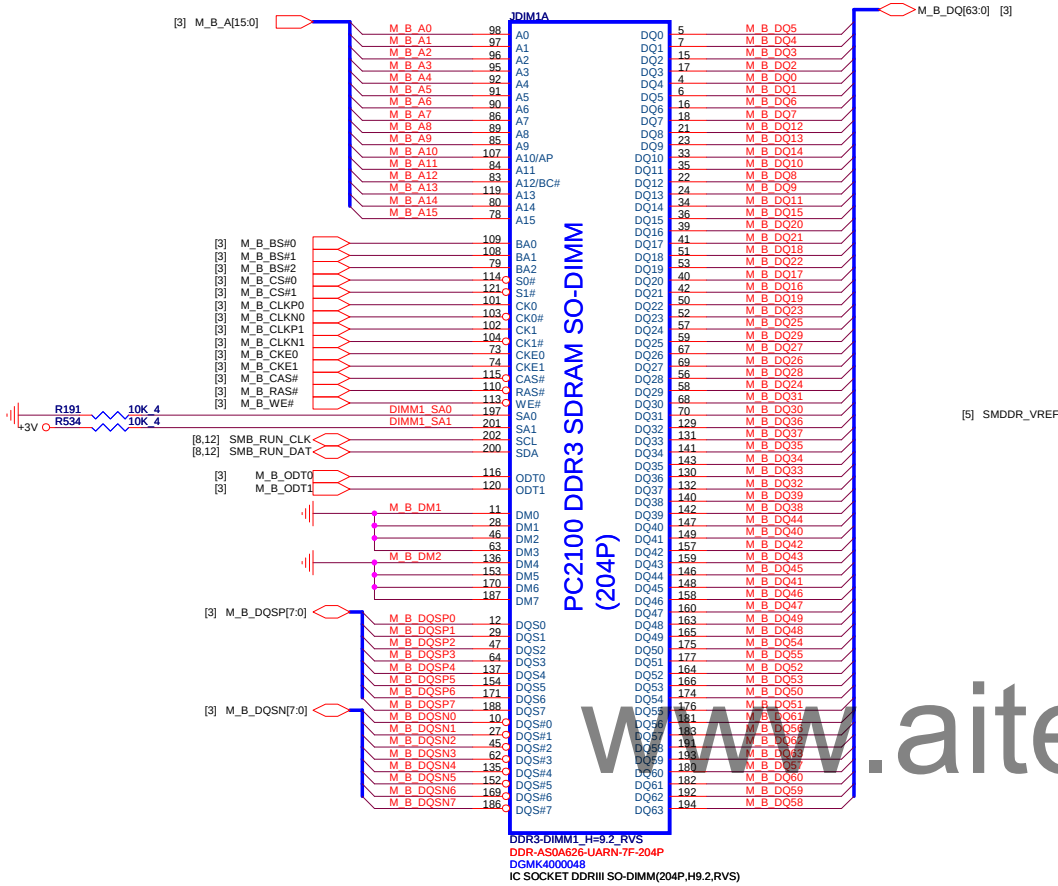
[2,6,7,8,9,10,13,14,21,22,23,24,25,26,27,28,29,30,31,32,38,40,41] +3V
[2,4,10,13,35,36,37,41] +1.5VSUS
[13,35,41] +0.75V_DDR_VTT
[13] +SMDDR_VREF_DIMM

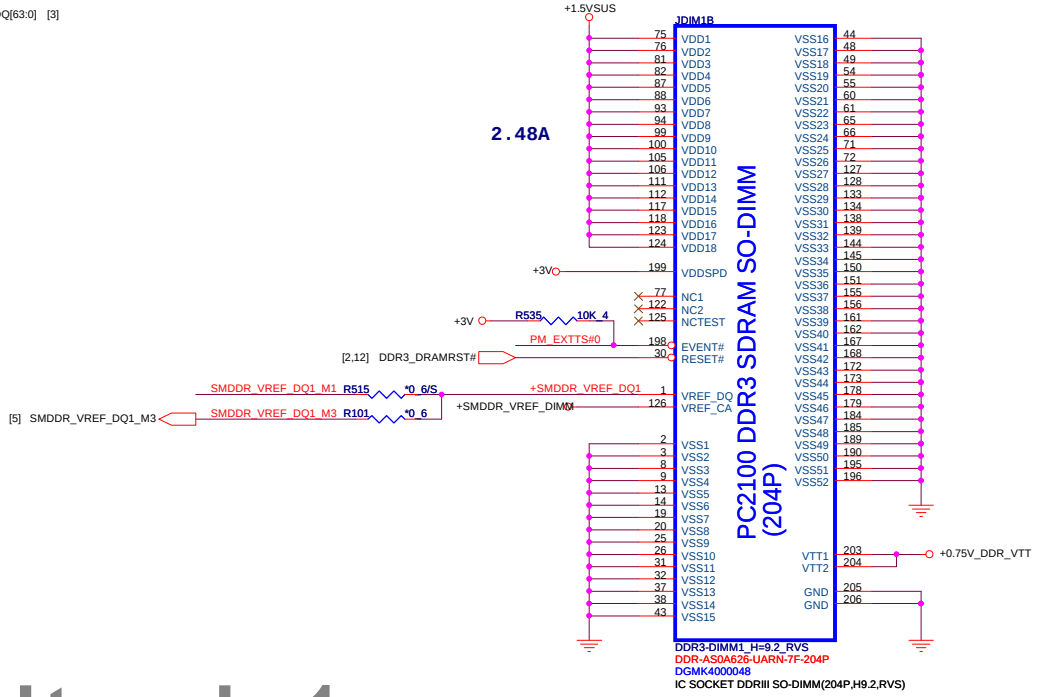
NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

Date: Friday, May 20, 2011 | Sheet 12 of 42





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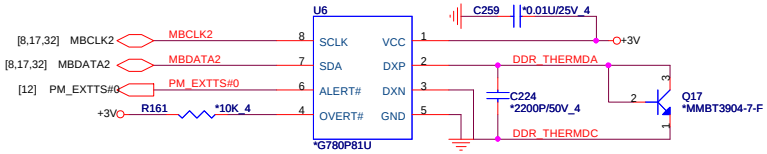
DDR3 Thermal Sensor

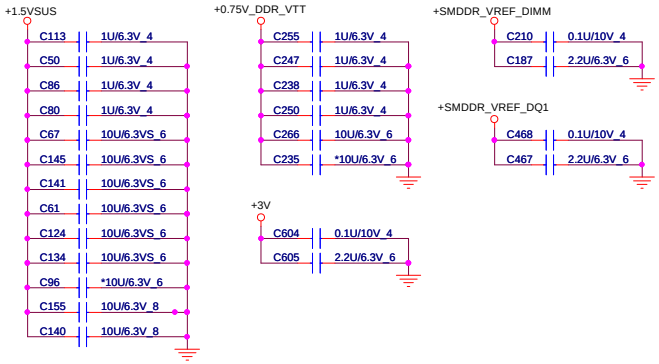


VREF DQ1 M2 Solution

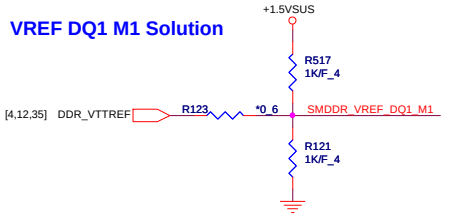
6/23 : Del M2 solution

4/29 reserve M2 solution

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



[2,6,7,8,9,10,12,14,21,22,23,24,25,26,27,28,29,30,31,32,38,40,41] +3V
[12] +SMDDR_VREF_DIMM
[2,4,10,12,35,36,37,41] +1.5VSUS
[12,35,41] +0.75V_DDR_VTT

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

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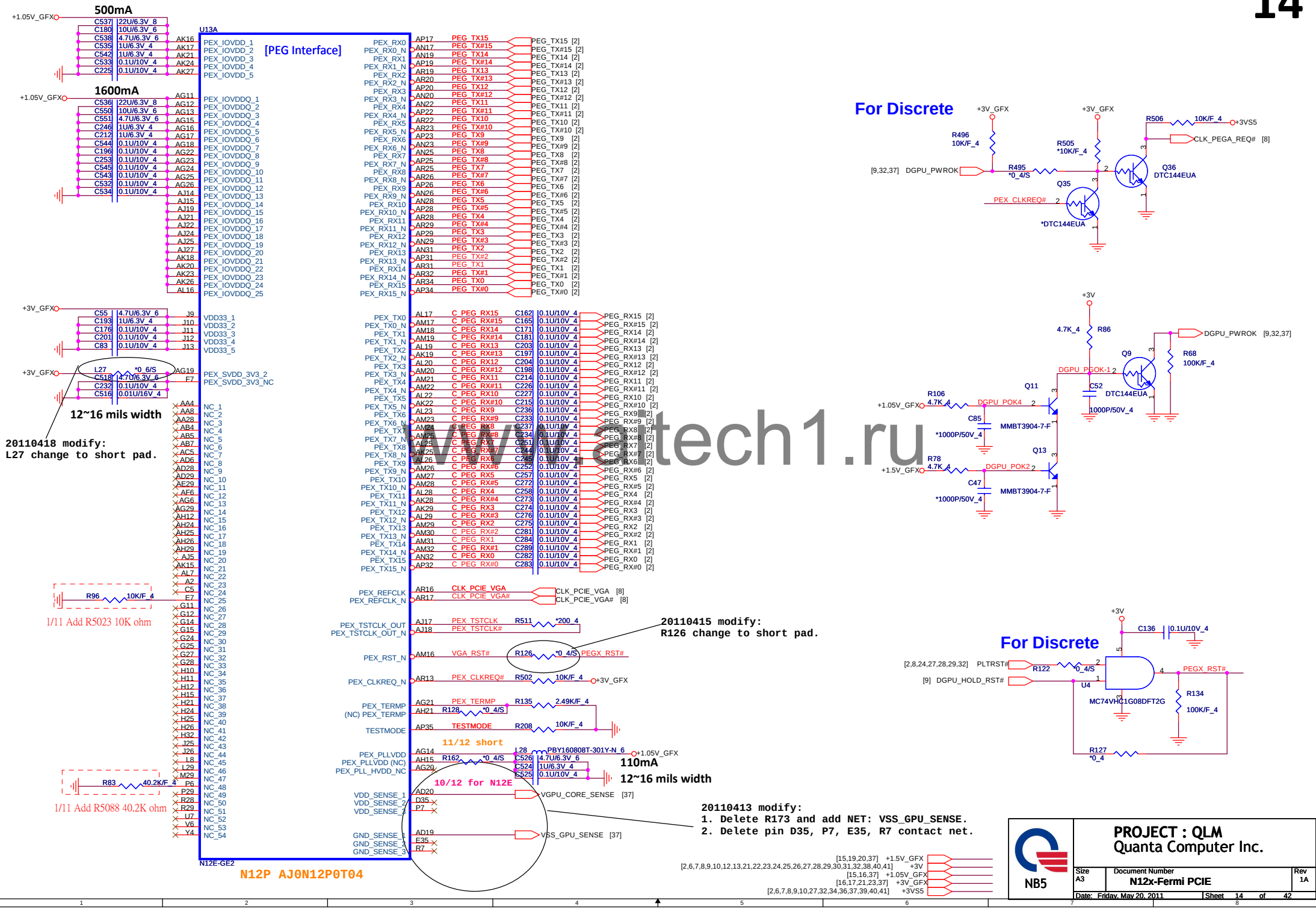

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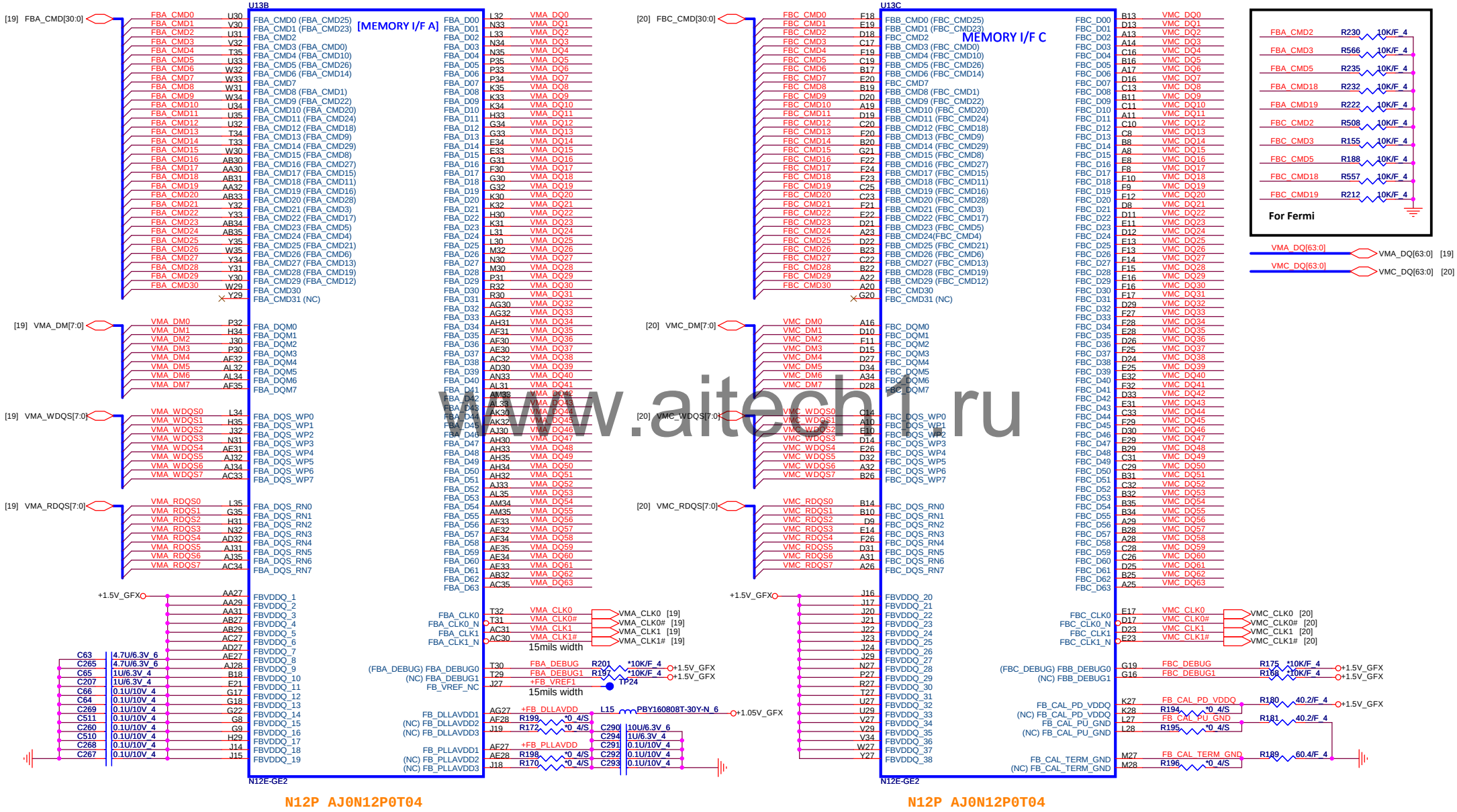
NB5	PROJECT : QLM Quanta Computer Inc.	
Size A3	Document Number N12x-Fermi PCIE	Rev 1A
Date: Friday, May 20, 2011	Sheet 14 of 42	



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PROJECT : QLM Quanta Computer Inc.		
NB5	Size A3	Document Number N12x-Fermi (MEM I/F) Rev 1A
	Date: Friday, May 20, 2011	Sheet 15 of 42

Optimus:
All unstuff , one Cap stuff 4.7K ohm

220 mA

+1.05V_GFX L10 *FBMA-10-160808-300T_6 +IFPAB_PLLVDD
R120 10K/F_4
C108 *4.7U/6.3V_6
C120 *0.1U/10V_4
C121 *1U/10V_4
1/11 Add C109 0.1uF and C127 1uF

R143 *1K/F_4 IFPAB_RSET

200 mA

+1.8V_VGA L6 *FBMA-10-160808-300T_6 +IFPAB_IOVDD
C84 *0.1U/10V_4
R99 10K/F_4
C68 *4.7U/6.3V_6
1/11 Add R59 0 ohm
R103 0_4
R125 10K/F_4

U13D

IFPAB_PLLVDD AK9
IFPAB_RSET AJ11
IFPA_IOVDD AG9
IFPB_IOVDD AG10
IFPA_IOVDD (NC) AH10
IFPB_IOVDD (NC) AH11

[IFPA/B_LVDS]

IFPA_TXC AM11 GPU_TXLCLKOUT+ → GPU_TXLCLKOUT+ [22]
IFPA_TXC_N AM12 GPU_TXLCLKOUT- → GPU_TXLCLKOUT- [22]
IFPA_TXD0 AM8 GPU_TXLOUT0+ → GPU_TXLOUT0+ [22]
IFPA_TXD0_N AL8 GPU_TXLOUT0- → GPU_TXLOUT0- [22]
IFPA_TXD1 AM10 GPU_TXLOUT1+ → GPU_TXLOUT1+ [22]
IFPA_TXD1_N AM9 GPU_TXLOUT1- → GPU_TXLOUT1- [22]
IFPA_TXD2 AK10 GPU_TXLOUT2+ → GPU_TXLOUT2+ [22]
IFPA_TXD2_N AL10 GPU_TXLOUT2- → GPU_TXLOUT2- [22]
IFPA_TXD3 AK11
IFPA_TXD3_N AL11

IFPB_TXC AP13 GPU_TXUCLKOUT+ → GPU_TXUCLKOUT+ [22]
IFPB_TXC_N AN13 GPU_TXUCLKOUT- → GPU_TXUCLKOUT- [22]
IFPB_TXD4 AN8 GPU_TXUOUT0+ → GPU_TXUOUT0+ [22]
IFPB_TXD4_N AP8 GPU_TXUOUT0- → GPU_TXUOUT0- [22]
IFPB_TXD5 AP10 GPU_TXUOUT1+ → GPU_TXUOUT1+ [22]
IFPB_TXD5_N AN10 GPU_TXUOUT1- → GPU_TXUOUT1- [22]
IFPB_TXD6 AR11 GPU_TXUOUT2+ → GPU_TXUOUT2+ [22]
IFPB_TXD6_N AR10 GPU_TXUOUT2- → GPU_TXUOUT2- [22]
IFPB_TXD7 AN11
IFPB_TXD7_N AP11

Optimus:
All unstuff , one Cap stuff 4.7K ohm

220 mA

+3V_GFX L9 *FBMA-10-160808-300T_6 +IFPCD_PLLVDD
C112 *0.1U/10V_4
C119 *0.1U/10V_4
C98 *0.1U/10V_4
C107 *4.7U/6.3V_6
C88 *1U/10V_4
1/19 Del R376
Add C102 0.1uF,C129 1uF

R124 1K/F_4 IFPCD_RSET
R482 *1K/F_4 DGPU_DAB_RSET

285 mA (1.05V +/- 3%)

+1.05V_GFX L8 *MLB-201209-0030P-N1-RU_8 +IFPCD_IOVDD
C115 *1U/10V_4
C133 *0.1U/10V_4
C122 *0.1U/10V_4
C109 *4.7U/6.3V_6
1/19 Del R385
Add C98 0.1uF,C128 1uF

IFPC_PLLVDD AJ9
IFPD_PLLVDD AC6
IFPC_RSET AK7
IFPD_RSET AB6
IFPC_IOVDD AJ8
IFPD_IOVDD AK8

[IFPC/D_TMDS]

IFPC_AUX_I2CW_SCL AP2 → HDMI_SCL [21]
IFPC_AUX_I2CW_SDA_N AN3 → HDMI_SDA [21]
IFPC_L0 AM7 N_TX2_HDMI+ → N_TX2_HDMI+ [21]
IFPC_L0_N AM6 N_TX2_HDMI- → N_TX2_HDMI- [21]
IFPC_L1 AL5 N_TX1_HDMI+ → N_TX1_HDMI+ [21]
IFPC_L1_N AM5 N_TX1_HDMI- → N_TX1_HDMI- [21]
IFPC_L2 AM3 N_TX0_HDMI+ → N_TX0_HDMI+ [21]
IFPC_L2_N AM4 N_TX0_HDMI- → N_TX0_HDMI- [21]
IFPC_L3 AP1 N_TXC_HDMI+ → N_TXC_HDMI+ [21]
IFPC_L3_N AR2 N_TXC_HDMI- → N_TXC_HDMI- [21]

IFPD_AUX_I2CX_SCL AP4
IFPD_AUX_I2CX_SDA_N AN4
IFPD_L0 AR8
IFPD_L0_N AR7
IFPD_L1 AP7
IFPD_L1_N AN7
IFPD_L2 AN5
IFPD_L2_N AP5
IFPD_L3 AR5
IFPD_L3_N AR4

Optimus:
All unstuff , one Cap stuff 4.7K ohm

AL1 IFPEF_RSET

R492 10K/F_4 IFPEF_PLLVDD
R489 10K/F_4 IFPEF_IOVDD

IFPEF_PLLVDD AJ6
IFPE_IOVDD AE7
IFPF_IOVDD AD7

[IFPE/F_DP]

IFPE_AUX_I2CY_SCL AE4
IFPE_AUX_I2CY_SDA_N AD4
IFPE_L0 AH6
IFPE_L0_N AH5
IFPE_L1 AH4
IFPE_L1_N AG4
IFPE_L2 AF4
IFPE_L2_N AF5
IFPE_L3 AE6
IFPE_L3_N AE5

IFPF_AUX_I2CZ_SCL AE3
IFPF_AUX_I2CZ_SDA_N AE2
IFPF_L0 AL2
IFPF_L0_N AL3
IFPF_L1 AJ3
IFPF_L1_N AJ2
IFPF_L2 AJ1
IFPF_L2_N AH1
IFPF_L3 AH2
IFPF_L3_N AH3

Optimus unstuff
For RGB , HYNC,VSYNC resistor

120 mA

+3V_GFX L11 *PBY160808T-301Y-N_6 +DACA_VDD
R104 10K/F_4
C102 *1U/10V_4
C91 *4.7U/6.3V_6
C127 *4700P/25V_4
C101 *0.1U/10V_4
C126 *0.1U/10V_4
C128 *0.1U/10V_4
C103 *0.1U/10V_4
1/11 Add C5040,C5043, C5053,C5073 0.1uF

C157 0.1U/10V_4 DACA_VREF
R133 124/F_4 DACA_RSET
R493 10K/F_4 DACB_VDD

DACA_VDD AJ12
DACA_VREF AK12
DACA_RSET AK13
DACB_VDD AG7

[DACA/B_CRT]

DACA_RED AM15 → R157 *150/F_4 → GPU_CRT_R [23]
DACA_GREEN AM14 → R151 *150/F_4 → GPU_CRT_G [23]
DACA_BLUE AL14 → R145 *150/F_4 → GPU_CRT_B [23]
DACA_HSYNC AM13 CRT_HSYNC R146 *33_4 → GPU_HSYNC [23]
DACA_VSYNC AL13 CRT_VSYNC R142 *33_4 → GPU_VSYNC [23]
I2CA_SCL G1 → GPU_DDCCLK [23]
I2CA_SDA G4 → GPU_DDCDATA [23]

+1.05V_GFX

L7 PBY160808T-30Y-N_6
C73 10U/6.3V_6
C77 0.1U/10V_4
C76 0.1U/10V_4
C75 0.1U/10V_4
C78 0.1U/10V_4

NV_PLLVDD R464 *0_4/S
SP_PLLVDD R465 *0_4/S
VID_PLLVDD R483 *0_4/S

AK6 DACB_VREF
AH7 DACB_RSET
PLLVDD AE9
PLLVDD (NC) AE8
SP_PLLVDD AF9
SP_PLLVDD (NC) AF8
VID_PLLVDD AD9
VID_PLLVDD (NC) AD8

DACB_RED AK4
DACB_GREEN AL4
DACB_BLUE AJ4
DACB_HSYNC AM1
DACB_VSYNC AM2
I2CB_SCL G3 N12E_SCL R76 2.2K_4 → +3V_GFX
I2CB_SDA G2 N12E_SDA R75 2.2K_4 → +3V_GFX

[XTAL IN]

XTAL_IN B1 CLK_27M_VGA_2
XTAL_OUT B2 XTALOUT
XTAL_OUTBUFF D1 R71 10K/F_4
XTAL_SSIN D2 R72 10K/F_4
Y3 27MHZ
C519 33P/50V_4
C520 33P/50V_4

N12E-GE2

N12P AJ0N12P0T04

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Power Sequence

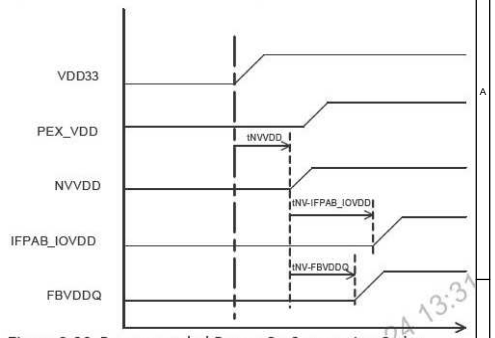


Figure 3.20 Recommended Power On Sequencing Order

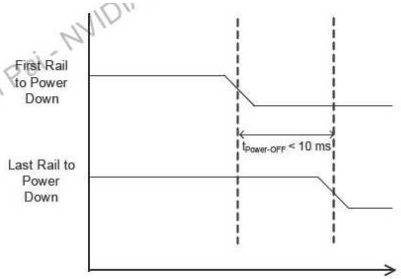


Figure 3.21 Recommended Power Off Sequencing Order

NVVDD Settling Time

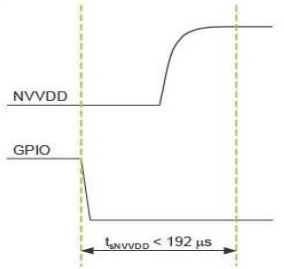


Figure 3.12 NVVDD Settling Time

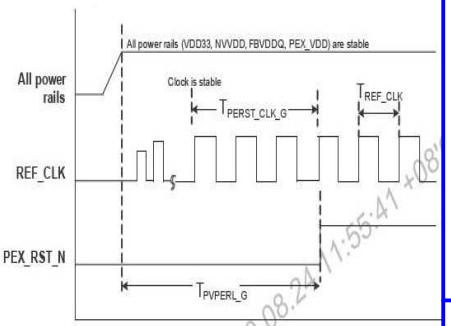
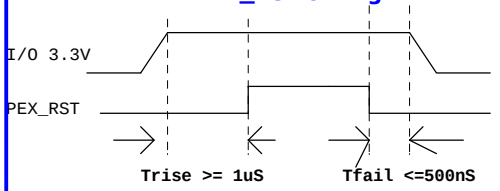


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL_G} \geq 1us$	
$T_{PERST_CLK_G}$	$T_{PERST_CLK_G} \geq 1T_{REF_CLK}$	

PEX_RST timing



[14,15,37] +1.05V_GFX
[14,17,21,23,37] +3V_GFX
[37] +1.8V_VGA

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
A3	N12x-Fermi (DISPLAY)	1A

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N12P-GVR device ID=0x1051
N12E-GE2 (LP sku)device ID=0x1248
N12E-GE2(Standard sku) device Id=0x1247

ROM_SI
Hynix 64Mx16 =15K PD
Samsung 64Mx16 =20K PD
Hynix 128Mx16 =35K PD
Samsung 128Mx16 =45K PD

ROM_SO
Both for N12E-GE2 & N12P-GVR
10K PD

ROM_SCLK
15K pull down for N12E-GE2
10K pull high for N12P-GVR

STRAP0
Both for N12E-GE2&N12P-GVR
45K pull high

STRAP1
Both for N12E-GE2&N12P-GVR
35K pull down

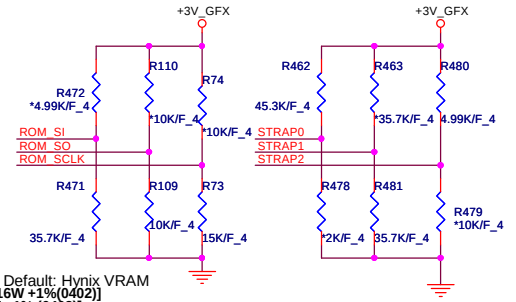
STRAP2
10K pull down for N12P-GVR
5K pull high for N12E-GE2 (LP sku)
45K pull down for N12E-GE2(Standard sku)

STRAP3
15K pull down for N12P-GVR.
Let it N.C for N12E-GE2.

STRAP4
10K pull down for N12P-GVR
Let it N.C for N12E-GE2.

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

Samsung 128Mx16

20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

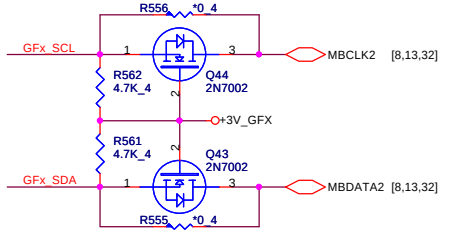
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

GFx SMBus Isolation



11/8 change for GPU temp detect

1/11 Add R5121,R5122 0 ohm
Add R5017 10K ohm
Add R5097 15K ohm

11/8 for N12E
11/12 short

N12P AJ0N12P0T04

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Quanta Computer Inc.

NB5

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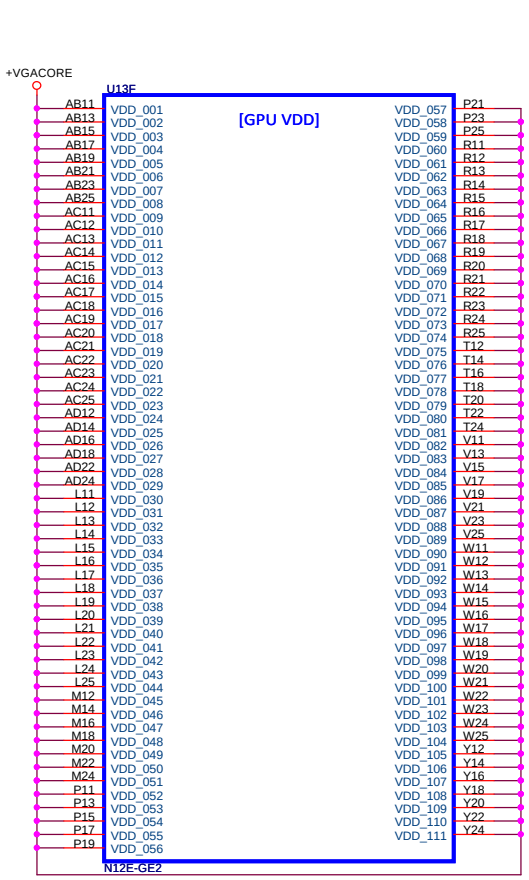
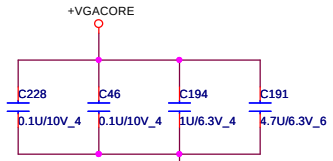
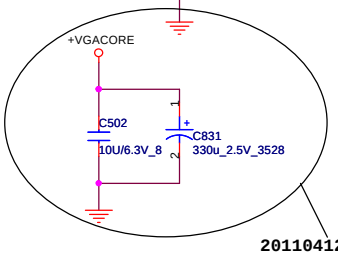
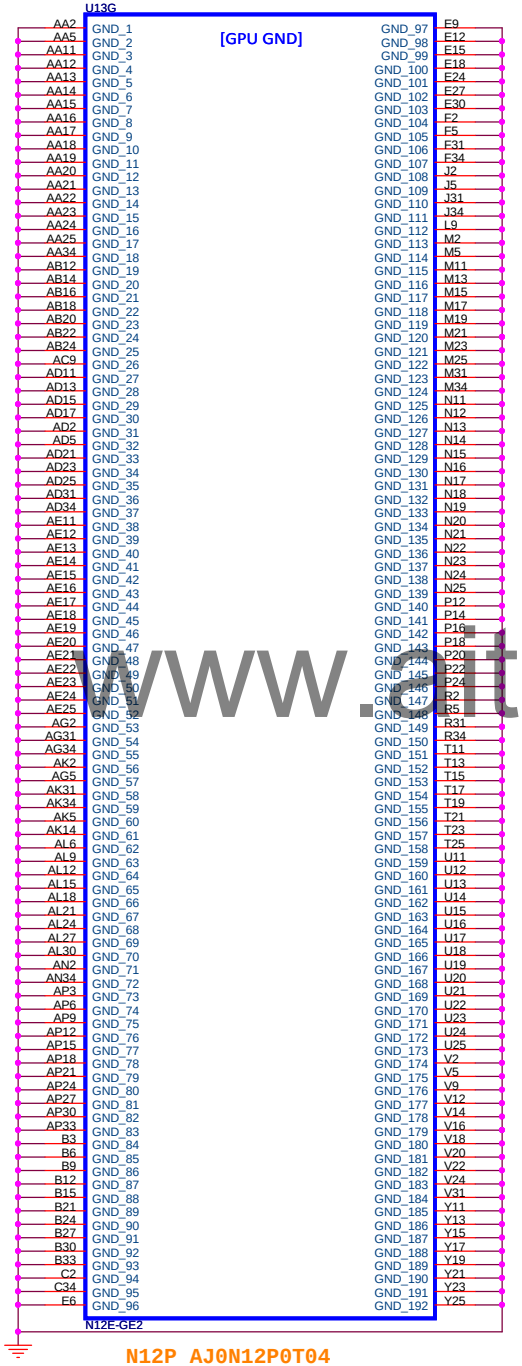


N12P AJ0N12P0T04



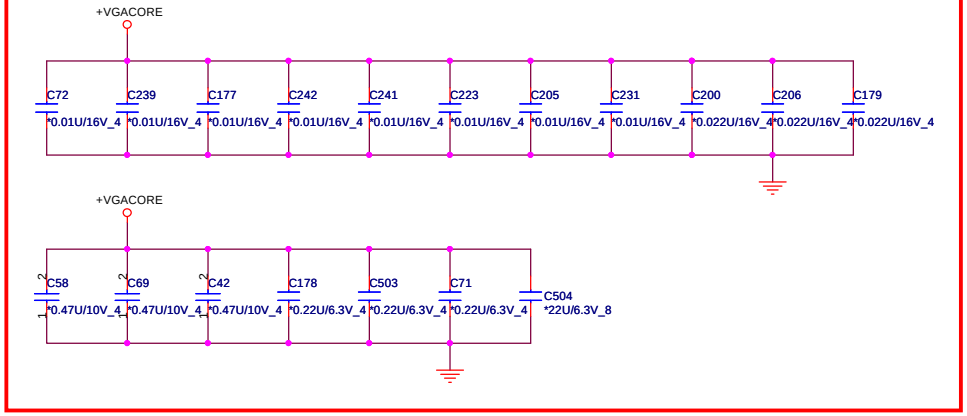


20110412 modify:
1. Delete C240, C209.
2. Add C831 330uF for reduce +VGACORE ripple noise.



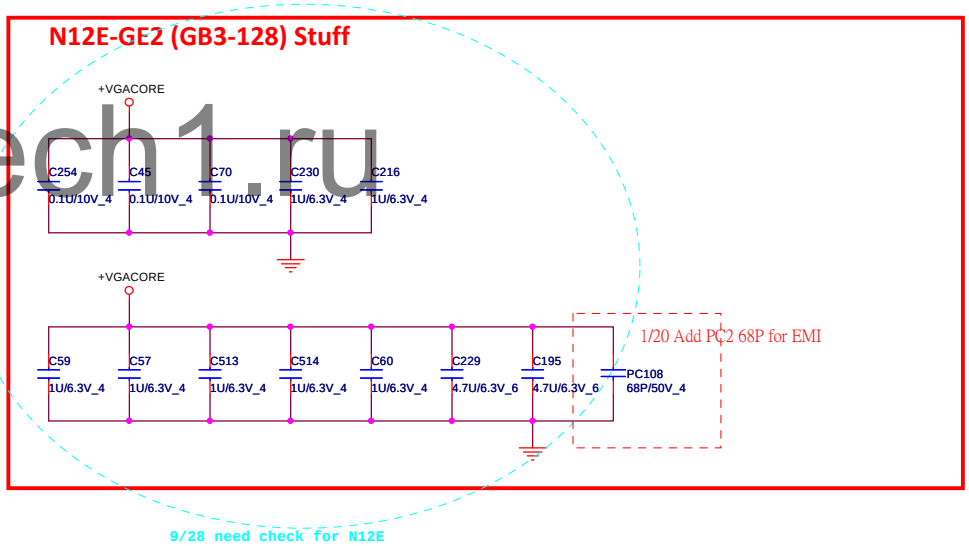
N12P AJ0N12P0T04

N12P-GS (GB2-128) Stuff



N12E-GE : C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411 stuff 0.1U/10V_4.
N12E-GE : C412 Stuff 47U/6.3V_8

N12E-GE2 (GB3-128) Stuff



9/28 need check for N12E

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[37] +VGACORE

NB5	PROJECT : QLM Quanta Computer Inc.	
Size A3	Document Number N12x-Fermi (GND/Power)	Rev 1A
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CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

VRAM3 / VRAM7 / VRAM4 / VRAM8
96-BALL SDRAM DDR3
VRAM_DDR3_HYNIX_128Mx16

Should be 240 Ohms +-1%
R224 243/F_4
R567 243/F_4
R223 243/F_4
R568 243/F_4

+1.5V_GFX

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK0 R221 158/F_4 VMA_CLK0#

R234 1.33K/F_4 VREFC_VMA1
R233 1.33K/F_4 C338 0.1U/10V_4
R228 1.33K/F_4 VREFD_VMA1
R226 1.33K/F_4 C336 0.1U/10V_4

[15] FBA_CMD17 FBA_CMD17 TP27
[15] FBA_CMD1 FBA_CMD1 TP28

VMA_CLK1 R220 158/F_4 VMA_CLK1#

R231 1.33K/F_4 VREFC_VMA3
R229 1.33K/F_4 C337 0.1U/10V_4
R227 1.33K/F_4 VREFD_VMA3
R225 1.33K/F_4 C335 0.1U/10V_4

C219 1U/10V_4
C303 1U/10V_4
C651 1U/10V_4
C642 1U/10V_4

C351 10U/6.3V_8
C356 0.1U/10V_4
C357 0.1U/10V_4
C304 0.1U/10V_4
C662 0.1U/10V_4
C354 0.1U/10V_4

C637 10U/6.3V_8
C643 0.1U/10V_4
C355 0.1U/10V_4
C339 0.1U/10V_4
C340 0.1U/10V_4
C346 0.1U/10V_4
C221 0.1U/10V_4
C341 0.1U/10V_4

C505 10U/6.3V_8
C656 10U/6.3V_8
C653 0.1U/10V_4
C661 0.1U/10V_4
C645 0.1U/10V_4
C650 0.1U/10V_4
C641 0.1U/10V_4

C644 10U/6.3V_8
C352 10U/6.3V_8
C648 0.1U/10V_4
C652 0.1U/10V_4
C649 0.1U/10V_4

[14,15,20,37] +1.5V_GFX

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12x-Fermi VRAM A	1A

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CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

VRAM5 / VRAM1 / VRAM2 / VRAM6
96-BALL SDRAM DDR3
VRAM _DDR3_HYNIX_128Mx16

Should be 240 Ohms +-1%
R460 243/F_4
R154 243/F_4
R211 243/F_4
R516 243/F_4

+1.5V_GFX

VMC_CLK0 — R89 158/F_4 — VMC_CLK0#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMC_CLK1 — R206 158/F_4 — VMC_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R458 1.33K/F_4 — VREFC_VMC1 — R459 1.33K/F_4 — C507 0.1U/10V_4
R152 1.33K/F_4 — VREFD_VMC1 — R153 1.33K/F_4 — C173 0.1U/10V_4
R209 1.33K/F_4 — VREFC_VMC3 — R210 1.33K/F_4 — C305 0.1U/10V_4
R165 1.33K/F_4 — VREFD_VMC3 — R166 1.33K/F_4 — C211 0.1U/10V_4

C142 C575 C353 C564 1U/10V_4
C172 C566 C208 10U/6.3V_8
C506 C508 C565 0.1U/10V_4
C218 C655 C220 C654 C657 C222 C174 C123 0.1U/10V_4
C217 C299 C302 C301 C300 C152 C509 C164 0.1U/10V_4

[15] FBC_CMD17 — FBC_CMD17 — TP22
[15] FBC_CMD1 — FBC_CMD1 — TP21

[14,15,19,37] +1.5V_GFX

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NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12x-Fermi VRAM B	1A

Date: Friday, May 20, 2011 | Sheet 20 of 42

20101117 modify:
Delete L48 / L49 / L50 / L51 for EMI.

L5 *DLP11SN900HL2L
N_TXC_HDMI+ 1 2 N_TXC_HDMI+
N_TXC_HDMI- 4 3 N_TXC_HDMI-

+5VCRT 40 mil R443 0_6 40 mil +5V_HDMVCC
C243 0.1U/10V_4

20110520 modify:
Q39, Q40 change from FDV301N to 2N7002.

20101117 modify:
R135, R136, R141, R142 change to 133 ohm for EMI.

EMI

C_TXC_HDMI+ R542 133/F_4 C_TXC_HDMI-
C_TX0_HDMI+ R530 133/F_4 C_TX0_HDMI-
C_TX1_HDMI+ R550 133/F_4 C_TX1_HDMI-
C_TX2_HDMI+ R559 133/F_4 C_TX2_HDMI-

HDMI_SDA_R R528 2.2K_4 2N7002K Q40 HDMI_SDATA R524 *0_4/S HDMI_SDATA_R
HDMI_SCL_R R507 2.2K_4 Q39 2N7002K HDMI_SCLK R512 *0_4/S HDMI_SCLK_R

Rb
R487 *0_4 +3V_GFX
HDMI_+3V
Ra
R485 0_4 +3V

UMA / Optimus：Ra stuff，Rb unstuff
DIS Only：Rb stuff，Ra unstuff

Ra
R657 0_4 +3V
R655 *0_4 +3V_GFX
Rb
Q48 MMBT3904-7-F HDMI_DET_P R651 150K/F_4 HDMI_HPD
HDMI_HPD_3V R658 10K_4 R652 *348K/F_4

D26 CH501H-40PT R513 2.2K_4
+5V_HDMVCC HI_PW5VC HI_PW5VD
D27 CH501H-40PT R523 2.2K_4
F2 FUSE1A6V_POLY +5V C571 0.1U/10V_4 +5V_HDMVCC

HDMI_SCLK_R HDMI_SDATA_R
HDMI_HPD R501 10K_4 HDMI_DET_N L29 BLM18BA470SN1D HDMI_DET_C
D24 *BAV99W +3V
R497 100K_4 C557 220P/50V_4

HDMI1
C_TX2_HDMI+ 1 D2+
C_TX2_HDMI- 2 D2 Shield
C_TX1_HDMI+ 3 D2-
C_TX1_HDMI- 4 D1+
C_TX0_HDMI+ 5 D1 Shield
C_TX0_HDMI- 6 D1-
C_TXC_HDMI+ 7 D0+
C_TXC_HDMI- 8 D0 Shield
9 D0-
10 CK+
11 CK Shield
12 CK-
13 CE Remote
14 NC
15 DDC CLK
16 DDC DATA
17 GND
18 +5V
19 HP DET
SHELL3 22
SHELL1 20
SHELL2 21
SHELL4 23
HDMI CONN_4 pin GND

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For UMA / Optimus HDMI function

[6] IN_CLK# C279 0.1U/10V_4 C_TXC_HDMI-
[6] IN_CLK C280 0.1U/10V_4 C_TXC_HDMI+
[6] IN_D0# C277 0.1U/10V_4 C_TX0_HDMI-
[6] IN_D0 C278 0.1U/10V_4 C_TX0_HDMI+
[6] IN_D1# C295 0.1U/10V_4 C_TX1_HDMI-
[6] IN_D1 C296 0.1U/10V_4 C_TX1_HDMI+
[6] IN_D2# C297 0.1U/10V_4 C_TX2_HDMI-
[6] IN_D2 C298 0.1U/10V_4 C_TX2_HDMI+
[6] SDVO_DATA SDVO_DATA R521 0_4 HDMI_SDA_R
[6] SDVO_CLK SDVO_CLK R519 0_4 HDMI_SCL_R
[6] HDMI_HPD_CON HDMI_HPD_CON R661 0_4 HDMI_HPD_3V

HDMI_+3V
Q42 2N7002K
R540 *100K_4 C610 *0.1U/10V_4

UMA / Optimus: 680 ohm
Discrete: 499 ohm

R560 680/F_4 C_TX2_HDMI+
R558 680/F_4 C_TX2_HDMI-
R554 680/F_4 C_TX1_HDMI+
R549 680/F_4 C_TX1_HDMI-
R532 680/F_4 C_TX0_HDMI+
R527 680/F_4 C_TX0_HDMI-
R546 680/F_4 C_TXC_HDMI+
R538 680/F_4 C_TXC_HDMI-

For DIS Only

[16] N_TX2_HDMI+ C288 *0.1U/10V_4 C_TX2_HDMI+
[16] N_TX2_HDMI- C287 *0.1U/10V_4 C_TX2_HDMI-
[16] N_TX1_HDMI+ C286 *0.1U/10V_4 C_TX1_HDMI+
[16] N_TX1_HDMI- C285 *0.1U/10V_4 C_TX1_HDMI-
[16] N_TX0_HDMI+ C264 *0.1U/10V_4 C_TX0_HDMI+
[16] N_TX0_HDMI- C263 *0.1U/10V_4 C_TX0_HDMI-
[16] N_TXC_HDMI+ C262 *0.1U/10V_4 C_TXC_HDMI+
[16] N_TXC_HDMI- C261 *0.1U/10V_4 C_TXC_HDMI-
[16] HDMI_SDA HDMI_SDA R520 *0_4 HDMI_SDA_R
[16] HDMI_SCL HDMI_SCL R518 *0_4 HDMI_SCL_R
[17] TMDS_HPD TMDS_HPD R662 *0_4 HDMI_HPD_3V

[2,6,7,8,9,10,12,13,14,22,23,24,25,26,27,28,29,30,31,32,38,40,41] +3V
[6,7,10,22,23,25,26,29,30,31,41] +5V
[14,16,17,23,37] +3V_GFX
[23] +5VCRT

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI and connector	1A
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UMA Optimus

[6] PCH_LA_CLK	PCH_LA_CLK	R61	0_4	TXLCLKOUT+
[6] PCH_LA_CLK#	PCH_LA_CLK#	R62	0_4	TXLCLKOUT-
[6] PCH_LA_DATAP0	PCH_LA_DATAP0	R64	0_4	TXLOUT0+
[6] PCH_LA_DATAN0	PCH_LA_DATAN0	R63	0_4	TXLOUT0-
[6] PCH_LA_DATAP1	PCH_LA_DATAP1	R44	0_4	TXLOUT1+
[6] PCH_LA_DATAN1	PCH_LA_DATAN1	R43	0_4	TXLOUT1-
[6] PCH_LA_DATAP2	PCH_LA_DATAP2	R45	0_4	TXLOUT2+
[6] PCH_LA_DATAN2	PCH_LA_DATAN2	R46	0_4	TXLOUT2-
[6] PCH_LB_CLK	PCH_LB_CLK	R65	0_4	TXUCLKOUT+
[6] PCH_LB_CLK#	PCH_LB_CLK#	R66	0_4	TXUCLKOUT-
[6] PCH_LB_DATAP0	PCH_LB_DATAP0	R41	0_4	TXUOUT0+
[6] PCH_LB_DATAN0	PCH_LB_DATAN0	R42	0_4	TXUOUT0-
[6] PCH_LB_DATAP1	PCH_LB_DATAP1	R59	0_4	TXUOUT1+
[6] PCH_LB_DATAN1	PCH_LB_DATAN1	R60	0_4	TXUOUT1-
[6] PCH_LB_DATAP2	PCH_LB_DATAP2	R53	0_4	TXUOUT2+
[6] PCH_LB_DATAN2	PCH_LB_DATAN2	R54	0_4	TXUOUT2-

DIS

[16] GPU_TXLCLKOUT+	GPU_TXLCLKOUT+	R51	*0_4	TXLCLKOUT+
[16] GPU_TXLCLKOUT-	GPU_TXLCLKOUT-	R52	*0_4	TXLCLKOUT-
[16] GPU_TXLOUT0+	GPU_TXLOUT0+	R56	*0_4	TXLOUT0+
[16] GPU_TXLOUT0-	GPU_TXLOUT0-	R55	*0_4	TXLOUT0-
[16] GPU_TXLOUT1+	GPU_TXLOUT1+	R36	*0_4	TXLOUT1+
[16] GPU_TXLOUT1-	GPU_TXLOUT1-	R35	*0_4	TXLOUT1-
[16] GPU_TXLOUT2+	GPU_TXLOUT2+	R37	*0_4	TXLOUT2+
[16] GPU_TXLOUT2-	GPU_TXLOUT2-	R38	*0_4	TXLOUT2-
[16] GPU_TXUCLKOUT+	GPU_TXUCLKOUT+	R57	*0_4	TXUCLKOUT+
[16] GPU_TXUCLKOUT-	GPU_TXUCLKOUT-	R58	*0_4	TXUCLKOUT-
[16] GPU_TXUOUT0+	GPU_TXUOUT0+	R32	*0_4	TXUOUT0+
[16] GPU_TXUOUT0-	GPU_TXUOUT0-	R33	*0_4	TXUOUT0-
[16] GPU_TXUOUT1+	GPU_TXUOUT1+	R49	*0_4	TXUOUT1+
[16] GPU_TXUOUT1-	GPU_TXUOUT1-	R50	*0_4	TXUOUT1-
[16] GPU_TXUOUT2+	GPU_TXUOUT2+	R47	*0_4	TXUOUT2+
[16] GPU_TXUOUT2-	GPU_TXUOUT2-	R48	*0_4	TXUOUT2-

UMA Optimus

[6] PCH_EDIDCLK	PCH_EDIDCLK	R414	0_4	EDIDCLK
[6] PCH_EDIDDATA	PCH_EDIDDATA	R411	0_4	EDIDDATA

+3V: R415 2.2K_4 PCH_EDIDCLK; R412 2.2K_4 PCH_EDIDDATA

DIS

[17] GPU_EDIDCLK	GPU_EDIDCLK	R115	*0_4	EDIDCLK
[17] GPU_EDIDDATA	GPU_EDIDDATA	R114	*0_4	EDIDDATA

UMA / Optimus

[6] PCH_LVDS_BLON	R394	0_4	LVDS_BLON	
[6] PCH_DISP_ON	R418	0_4	DISP_ON	
[6] PCH_DPST_PWM	R406	0_4	DPST_PWM	

DIS

[17] GPU_LVDS_BLON	R395	*0_4	LVDS_BLON	
[17] GPU_DISP_ON	R417	*0_4	DISP_ON	
[17] GPU_DPST_PWM	R405	*0_4	DPST_PWM	

20110415 modify:
R399 change to short pad.

[32] LID_CONTROL — R399 *0_4/S_PN — BLON — D19 RB501V-40 — R401 100K/F_4 — C457 22P/50V_4 — BLON_CON

LVDS_BLON — R398 1K/F_4 — D20 *RB501V-40 — R400 47K_4 — +3VPCU — LID_EC# [31,32]

R397 100K/F_4

[8] LCD_BK — Q27 *DTC144EUA

+VIN — L1 UPB201209T-330Y-N — +VIN_BLIGHT

C1 *.1U/50V_6; C455 .1U/50V_6; C5 .01U/25V_4; C2 .1U/50V_6; C4 *10U/25V_12

EDIDCLK, EDIDDATA — C26 10P/50V_4; C27 10P/50V_4

20110519 modify:
C26 and C27 change from reserve to 10pF for EMI.

+3VLCD_CON — CN1 *DFHS04FS969

Webcam
8/23 A-->B update.

DIGITAL_D1, DIGITAL_CLK_L — C8 10P/50V_4; C20 10P/50V_4

8/27 Add C8,C11 for EMI issue

+3VLCD_CON — C469 1000P/50V_4 — +3V

EDIDCLK, EDIDDATA, TXLOUT0-, TXLOUT0+, TXLOUT1-, TXLOUT1+, TXLOUT2-, TXLOUT2+, TXLCLKOUT-, TXLCLKOUT+, TXUOUT0-, TXUOUT0+, TXUOUT1-, TXUOUT1+, TXUOUT2-, TXUOUT2+, TXUCLKOUT-, TXUCLKOUT+

L3 SBK160808T-601Y-N

[25] DIGITAL_D1 — L2 SBK160808T-601Y-N — DIGITAL_D1_CN

[25] DIGITAL_CLK — DIGITAL_CLK_L

[8] USBP9- — L4 WCM2012-90 — USBP9-_L

[8] USBP9+ — USBP9+_L

+3.9V_CAM

[32] PWM_VADJ — R3 *0_4 — DPST_PWM — BLON_CON

8/30 Change netname from USBP9- to USBP9-_L
Change netname from USBP9+ to USBP9+_L

+VIN_BLIGHT — C459 22P/50V_4

LVDS1 GS12401-1011-9F

LVDS_BLON — R396 *100K/F_4

DISP_ON — R420 *100K/F_4

20101116 modify:
R296, R321 un-stuff for repeat pull down.

14.5v

20100623 modiy:
+5VSUS change to +5V_S5

+12VALW — R413 330K_6 — Q29 AO3404 — LCDON — +3V — C472 0.1U/10V_4 — +3VLCD

+5VS5 — R408 100K/F_4

Q30 2N7002E — C476 .027U/25V_6 — LCDON#

Q31 DTC144EUA — DISP_ON — R419 100K/F_4

Q28 2N7002E — LCDDISCHG — R410 22_8

+3VLCD_CON — L23 HCB2012KF-600T30 — C474 .01U/25V_4; C475 0.1U/10V_4; C466 10U/6.3V_8

+3VPCU — C456 *0.1U/10V_4

+5V — L22 HCB2012KF-600T30 — +3.9V_CAM

C462 10U/6.3V_8; C458 0.01U/16V_4

[10,28,31,34,35,36,37,38,39,40,41] +5VS5
[2,6,7,8,9,10,12,13,14,21,23,24,25,26,27,28,29,30,31,32,38,40,41] +3V
[6,7,10,21,23,25,26,29,30,31,41] +5V
[33,34,35,36,37,38,39,41] +VIN
[6,7,31,32,33,34,41] +3VPCU
[30,37,41] +12VALW

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	1A

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CRT PORT

+5VCRT C492 0.1U/10V_4

+5V F1 40 mils 40 MIL +5VCRT

*FUSE1A6V_POLY SSM14 spec is 40V 1A

8/27 modify L6 , L7, L8 to 47 ohm

CRT_R_CON L24 BLM18BA470SN1(0.3A,47)_6 CRT_R1

CRT_G_CON L25 BLM18BA470SN1(0.3A,47)_6 CRT_G1

CRT_B_CON L26 BLM18BA470SN1(0.3A,47)_6 CRT_B1

R446 150/F_4 R447 150/F_4 R448 150/F_4

C499 5.6P/16V_4 C500 5.6P/16V_4 C501 5.6P/16V_4

C497 5.6P/16V_4 C496 5.6P/16V_4 C498 5.6P/16V_4

CRT CONN CRT1

+3V C43 0.1U/10V_4 +5V C495 0.1U/10V_4

CRTVSYNC_1 R22 22_4 CRTVSYNC_2

CRTHSYNC_1 R29 22_4 CRTHSYNC_2

DDCCLK_COM Q10 2N7002E DDCCLK2 R82 22_4 DDCCLK3

+3V Q8 2N7002E DDCDAT2 R79 22_4 DDCDAT3

DDCDATA_COM

C49 *470P/50V_4 C29 10P/50V_4 C38 *47P/50V_4 C44 10P/50V_4

R81 2.2K_4 R80 2.2K_4

U2 M74VHC1GT125DF2G

VSYNC_COM CRTVSYNC_1

HSYNC_COM CRTHSYNC_1

U3 M74VHC1GT125DF2G

+5VCRT D4 RB501V-40 +5V_CRT2

C494 0.22U/6.3V_4

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20100427 modify:
R73, R74, R75, R70, R71, R72 change to 0 ohm.

UMA / Optimus

[6] PCH_CRT_R PCH_CRT_R R457 0_4 CRT_R_CON

[6] PCH_CRT_G PCH_CRT_G R453 0_4 CRT_G_CON

[6] PCH_CRT_B PCH_CRT_B R455 0_4 CRT_B_CON

[6] PCH_HSYNC PCH_HSYNC R92 BLM15BB221SN1D HSYNC_COM

[6] PCH_VSYNC PCH_VSYNC R90 BLM15BB221SN1D VSYNC_COM

[6] PCH_DDCCLK PCH_DDCCLK R77 0_4 DDCCLK_COM

[6] PCH_DDCDATA PCH_DDCDATA R432 0_4 DDCDATA_COM

+3V R67 4.7K/F_4 PCH_DDCCLK R424 4.7K/F_4 PCH_DDCDATA

DIS Only

[16] GPU_CRT_R GPU_CRT_R R450 *0_4 CRT_R_CON

[16] GPU_CRT_G GPU_CRT_G R454 *0_4 CRT_G_CON

[16] GPU_CRT_B GPU_CRT_B R456 *0_4 CRT_B_CON

[16] GPU_HSYNC GPU_HSYNC R93 *BLM15BB221SN1D HSYNC_COM

[16] GPU_VSYNC GPU_VSYNC R91 *BLM15BB221SN1D VSYNC_COM

[16] GPU_DDCCLK GPU_DDCCLK R70 *0_4 DDCCLK_COM

[16] GPU_DDCDATA GPU_DDCDATA R431 *0_4 DDCDATA_COM

DIS Only / Optimus stuff

+3V_GFX R69 4.7K/F_4 GPU_DDCCLK R423 4.7K/F_4 GPU_DDCDATA

PCH_CRT_R PCH_CRT_G PCH_CRT_B

C381 *5.6P/16V_4 C380 *5.6P/16V_4 C384 *5.6P/16V_4

[21] +5VCRT

[14,16,17,21,37] +3V_GFX

[6,7,10,21,22,25,26,29,30,31,41] +5V

[2,6,7,8,9,10,12,13,14,21,22,24,25,26,27,28,29,30,31,32,38,40,41] +3V

ESD PROTECTION

D23 BAV99W CRT_B1

D22 BAV99W CRT_G1

D21 BAV99W CRT_R1

D2 BAV99W CRTVSYNC_2

D3 BAV99W CRTHSYNC_2

D8 BAV99W DDCCLK3

D5 BAV99W DDCDAT3

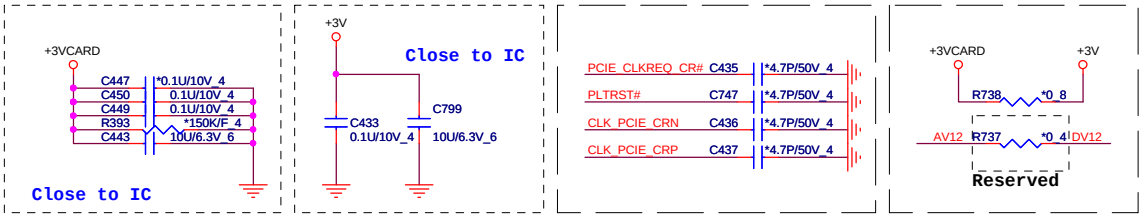
20100422 modify:
D22, D23, D24, D25 stuff for LG request.

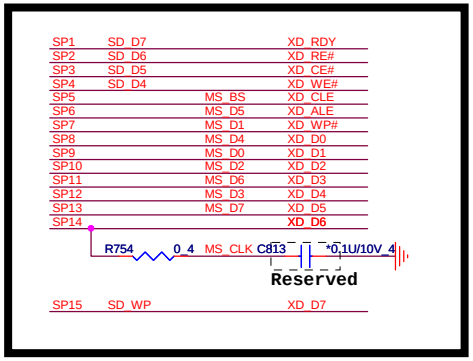
NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A

Date: Friday, May 20, 2011 Sheet 23 of 42





20110519 modify:
1. R385 change from 33 to 0 ohm for EMI.
2. R386 change from 0 to 33 ohm for EMI.
3. C446 change from reserve to 10pF for EMI.

7-in-1
flash media
slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)

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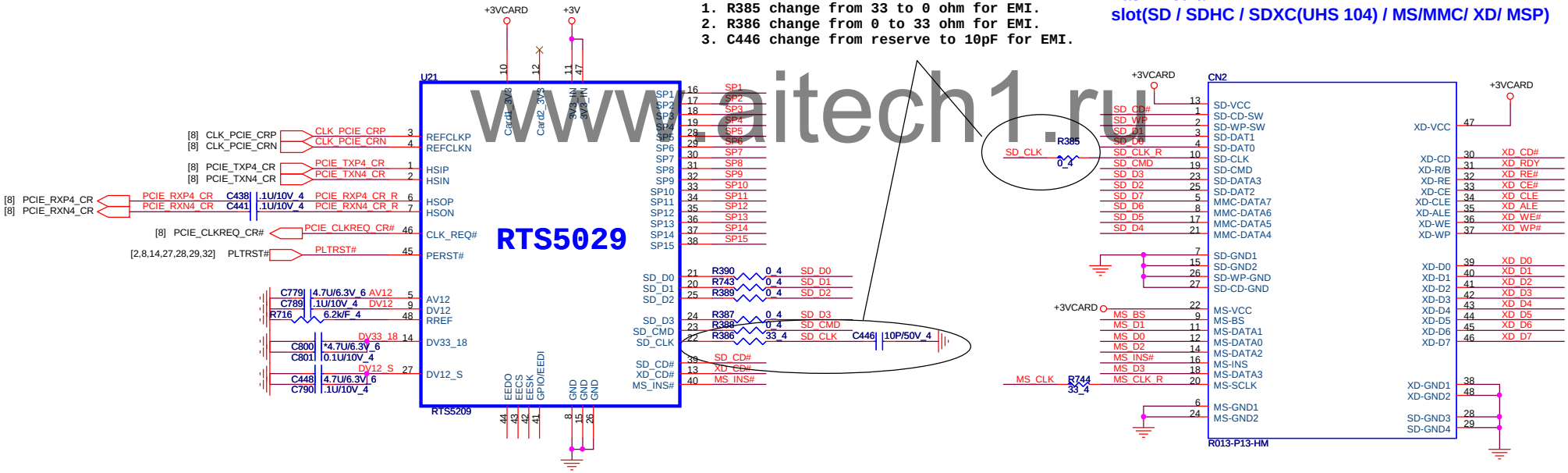


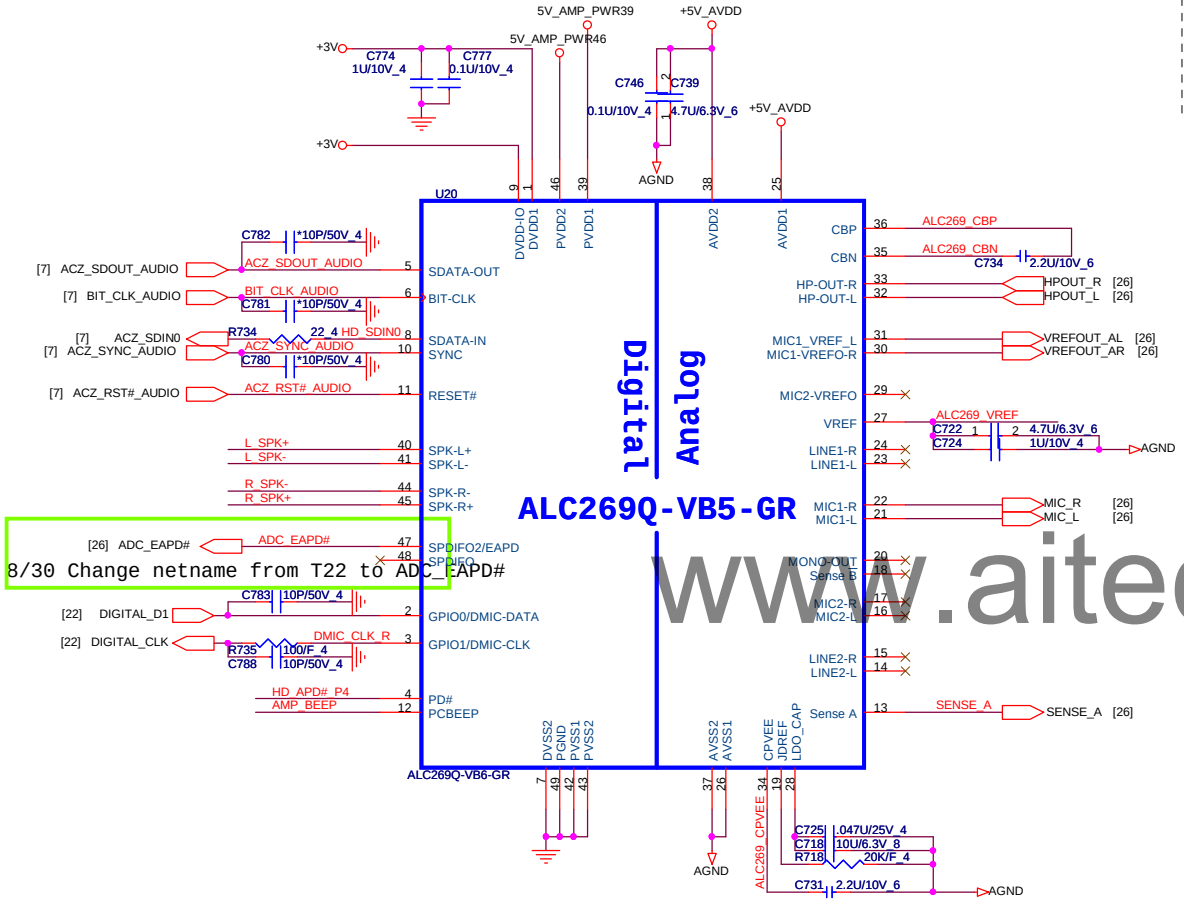
20110412 modify:
1. CN2 modify 4 pin GND CONN for EMI.

[2,6,7,8,9,10,12,13,14,21,22,23,25,26,27,28,29,30,31,32,38,40,41] +3V

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card reder (RTS5029)	1A
Date: Friday, May 20, 2011	Sheet 24 of 42	



8/30 Change netname from T22 to ADC_EAPD#

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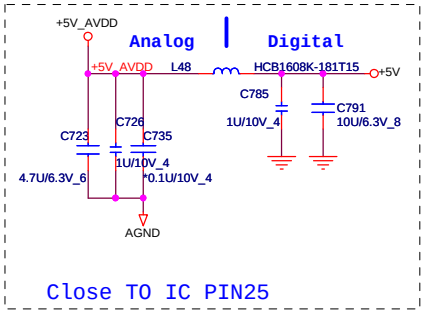
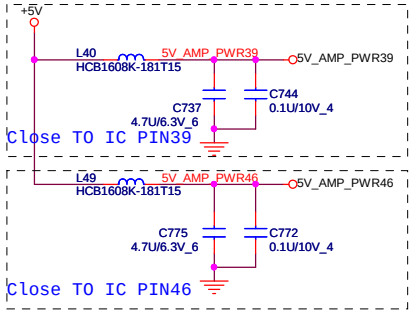
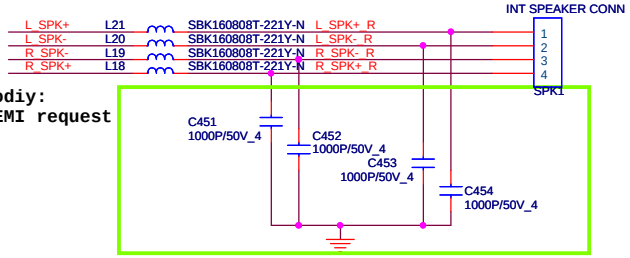
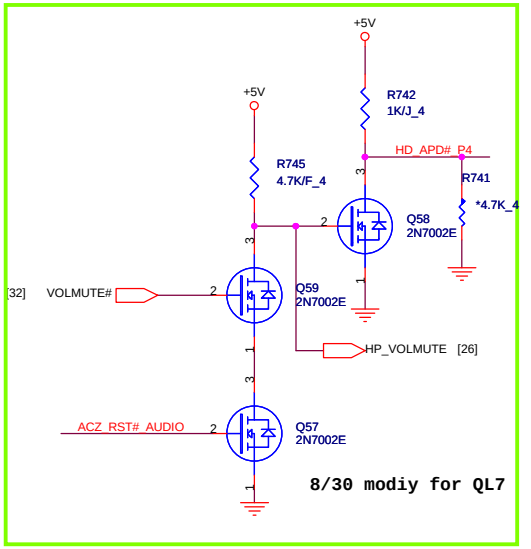




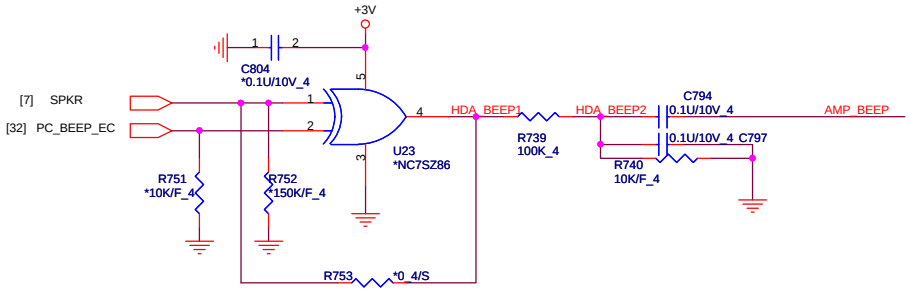
INT. SPEAKER

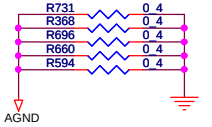


20100824 modiy:
mount for EMI request



8/30 modiy for QL7





[6,7,10,21,22,23,26,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,21,22,23,24,26,27,28,29,30,31,32,38,40,41] +3V

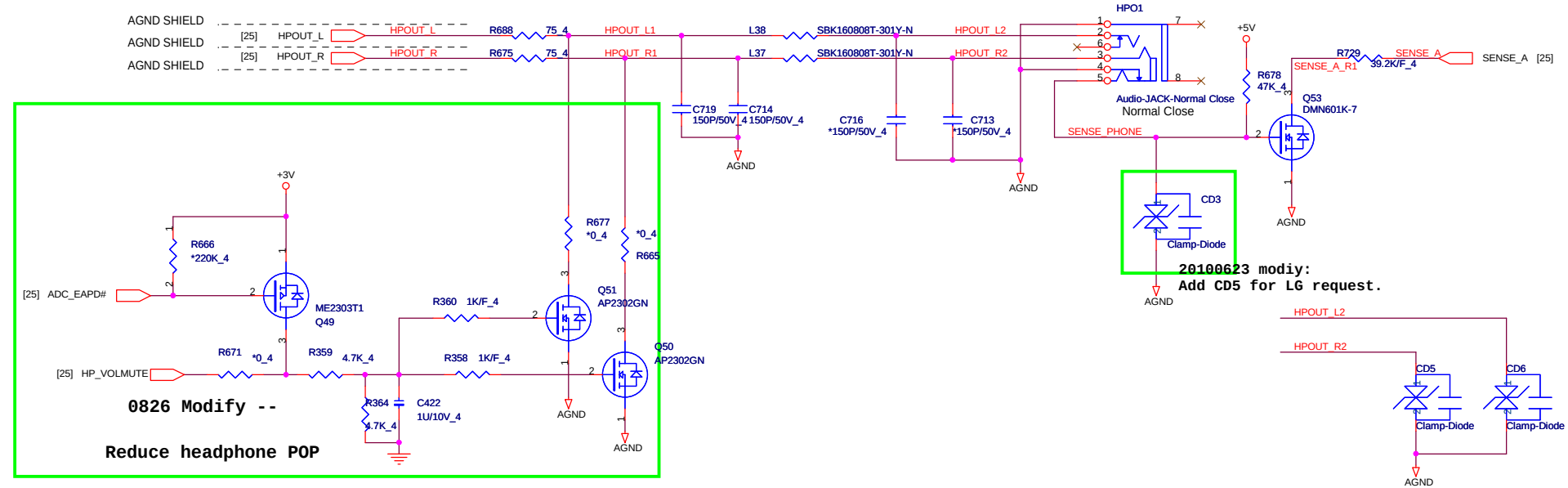
NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDA Azalia ALC269	1A

Date: Friday, May 20, 2011 Sheet 25 of 42

Line out



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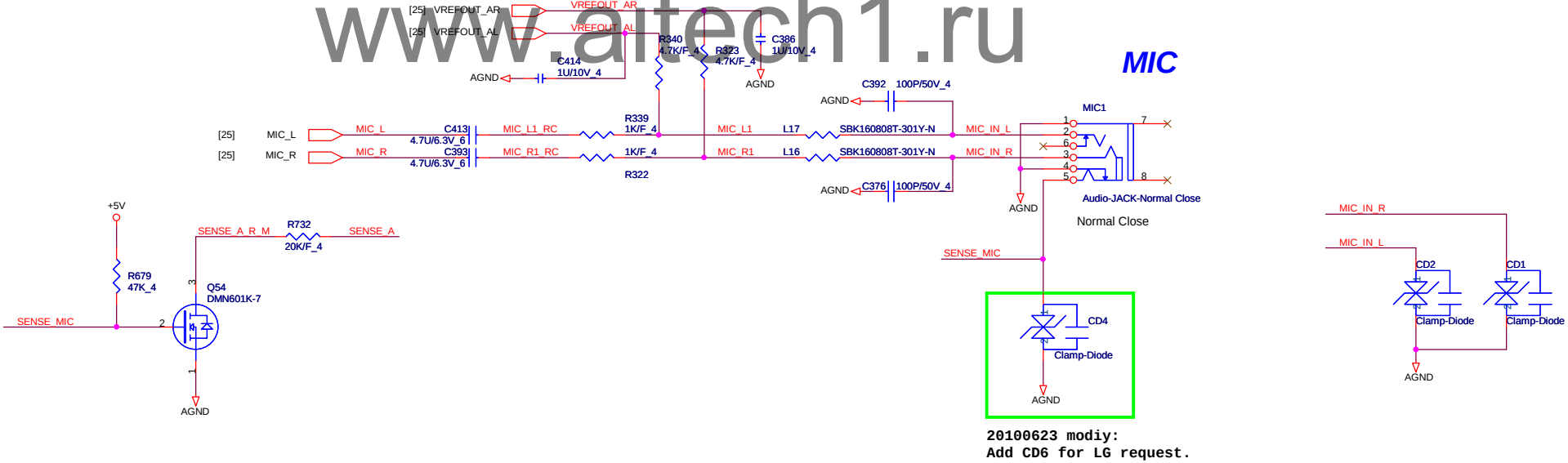
MIC



[6,7,10,21,22,23,25,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,30,31,32,38,40,41] +3V

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio Jack/Accelerometer	1A

Date: Friday, May 20, 2011 | Sheet 26 of 42

Atheros Lan

8/27 Add R139 for LAN POWER issue

+3VS5 — R302 *0_6 — +3VLANVCC

PLACE NEAR LAN IC PIN6

AVDDL C363 1U/6.3V_4
AVDDL C361 0.1U/10V_4
C369 10U/6.3V_8
C370 10U/6.3V_8
C372 1000P/50V_4
C368 1U/6.3V_4
C367 0.1U/10V_4
AVDDL C670 0.1U/10V_4
AVDDL C668 0.1U/10V_4
AVDDL C688 0.1U/10V_4
AVDDL C689 0.1U/10V_4

U7 — **Atheros AR8151** (AR8151-AL1A)

[8] CLK_PCIE_LANP — R617 *0_4/S — REFCLKP
[8] CLK_PCIE_LANN — R618 *0_4/S — REFCLKN
[8] PCIE_RXP2_LAN — C687 0.1U/10V_4 PCIE_RXP2_LAN_L — TX_P
[8] PCIE_RXN2_LAN — C683 0.1U/10V_4 PCIE_RXN2_LAN_L — TX_N
[8] PCIE_TXP2_LAN — RX_P
[8] PCIE_TXN2_LAN — RX_N

[2,8,14,24,28,29,32] PLTRST# — PERSTn
[6,28] PCIE_WAKE# — R573 *0_4/S — D28 RB501V-40 R — PCIE_WAKE# R — WAKEn
C365 *0.1U/10V_4 CKREQ_G# — VDDCT_REG/CKRn
R244 2.37K/F_4 — LANRSET — RBIAS
+3VLANVCC — R591 *4.7K_4 — R597 *4.7K_4 — SMCLK / SMDATA

TRXP0 MDI0+ / TRXN0 MDI0- / TRXP1 MDI1+ / TRXN1 MDI1- / TRXP2 MDI2+ / TRXN2 MDI2- / TRXP3 MDI3+ / TRXN3 MDI3-
LED_LINK10/100n LAN_GLINK100# / LED_ACTn LAN_TX# / CLKREQn/LED2 CKREQ#
LX — L34 4.7uh_C_1A — C692 0.1U/10V_4, C693 0.1U/10V_4, C694 10U/6.3V_8, C691 1000P/50V_4, C364 0.1U/10V_4
VDDCT — AVDD_CEN
TEST_RST, TESTMODE, GND1

XTLO — LAN_XTAL2 — Y2 — XTLI — LAN_XTAL1
C360 33P/50V_4 — 25MHZ — C359 33P/50V_4

C690 1U/6.3V_4, C686 0.1U/10V_4 DVDDL, C666 0.1U/10V_4 DVDDL
AVDDH C664 1U/6.3V_4, C663 0.1U/10V_4, AVDDH C667 0.1U/10V_4, AVDDH C669 0.1U/10V_4

C148 *6.8P/50V_4 LAN_MX1-
C149 *6.8P/50V_4 LAN_MX1+
C170 *6.8P/50V_4 LAN_MX0-
C188 *6.8P/50V_4 LAN_MX0+

GIGA LAN ONLY

+3V — Q21 2N7002E — +3VLANVCC — R616 4.7K_4
[8] PCIE_CLKREQ_LAN# — R592 *0_4 CKREQ_G# — Ra — R590 *0_4 CKREQ# — Rb
R620 *0_4 AVDD_CEN — Rc
C673 *1U/6.3V_4, C685 *0.1U/10V_4, C682 *10U/6.3V_8

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

RJ45C1 — JM36111-R6521-7F

LAN_TX# — R491 330/F_4 — LAN_TX# C — C522 1000P/50V_4 — LAN_MX3-
LAN_MX3+
LAN_MX1-
LAN_MX2-
LAN_MX2+
LAN_MX1+
LAN_MX0-
LAN_MX0+
NC4/3- / NC/3+ / RX-/1- / NC2/2- / NC1/2+ / RX+/1+ / TX-/0- / TX+/0+ / GND / GND / GND / GND / G- / G+

LAN_TX# R494 5.1K/F_6
LAN_GLINK100# C — C199 1000P/50V_4
LAN_GLINK100# — D25 RB501V-40 — R498 330/F_4 — +3VLANVCC — LAN_GLINK100# C — C553 1000P/50V_4

LAN_GLINK100#
LAN_TX#
C528 1000P/50V_4 — C541 1000P/50V_4

PLACE NEAR LAN IC SIDE

C343 1000P/50V_4 R237 49.9/F_4 MDI0+ / MDI0-
C342 0.1U/10V_4 R236 49.9/F_4
C345 1000P/50V_4 R239 49.9/F_4 MDI1+ / MDI1-
C344 0.1U/10V_4 R238 49.9/F_4
C350 1000P/50V_4 R243 49.9/F_4 MDI2+ / MDI2-
C349 0.1U/10V_4 R242 49.9/F_4
C348 1000P/50V_4 R241 49.9/F_4 MDI3+ / MDI3-
C347 0.1U/10V_4 R240 49.9/F_4

TRANSFORMER

C660 1U/6.3V_4 — TRA_V_DAC — L32 PBY160808T-601Y-N_1A — AVDD_CEN

U15 — NS892405

MDI0+ / MDI0- / MDI1+ / MDI1- / MDI2+ / MDI2- / MDI3+ / MDI3-
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-
LAN_MX0+ / LAN_MX0- / LAN_MX1+ / LAN_MX1- / LAN_MX2+ / LAN_MX2- / LAN_MX3+ / LAN_MX3-

TRA_V_DAC ×4
TCT1 TCT2 TCT3 TCT4 / MCT1 MCT2 MCT3 MCT4
LAN_MCTG0 R219 75/F_4 / LAN_MCTG1 R218 75/F_4 / LAN_MCTG2 R217 75/F_4 / LAN_MCTG3 R216 75/F_4 — LAN_MCTG — Re Rd

C659 *1000P/50V_4 0.1U/10V_4
C658 *1000P/50V_4 0.1U/10V_4
C678 0.1U/10V_4
C684 *1000P/50V_4 0.1U/10V_4
C675 *1000P/50V_4 0.1U/10V_4
C665 *1000P/50V_4 0.1U/10V_4
C672 *1000P/50V_4 0.1U/10V_4
C671 *1000P/50V_4 0.1U/10V_4

C639 10P/3KV_1808

D3A: only UMA sku support 1G,If support 10/100 in UMA SKU, R55,R56 change to 0-ohm

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NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN AR8151/RJ45	1A

Date: Friday, May 20, 2011 — Sheet 27 of 42

20110418 modify:
R711 change to short pad.

20110415 modify:
1. CN5 change footprint for SMT issue.
2. Add D32 for USB 3.0 ESD.
3. Stuff C647 and C646 for USB 2.0 ESD

20110418 modify:
R769 change to short pad.

20110415 modify:
1. R762 change from 4.7K to 1K for S3 issue.

20110519 modify:
Add RP7 for EMI.

20110412 modify:
Add NET Charger_ON and R774 to U16 Pin5

20110519 modify:
Add R335, R776, R353 for reserve TPS2543.

20110415 modify:
1. Add C209 for S3 issue.
2. Reserve R775.

VIA VL801

U22

PORT1 PORT2 PORT3 PORT4

USB3.0/USB2.0 x1 COMBO

USB 3.0/USB2.0

D32 SP3010-04UTG

CN5 USB3.0 CONN

CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode (SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define and wake up		SDP		OFF

Charger USB

high active
80 mils (Iout=2A)

Ios = 48000/RILIM0
default: Auto-detect

200mills

To Host

1/20 Del netname SPICS#,SPISO,SPISI,SPISCLK

1/20 Del netname USB_HPE#

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PROJECT : QLM
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	USB 3.0 Controller (VIA_VL801)	1A
Date: Friday, May 20, 2011	Sheet 28 of 42	

Mini PCI-E Card 1 - Half WLAN

20101123 modify:
R164 un-stuff for Intel QS combo card.

Ra = 0 ohm, INTEL ES Rev. combo card
Ra = un-stuff, INTEL QS Rev.combo card.

20101122 modify:
R82 change short pad.

9/2 change netname from TACH0 to RF_PWR_OFF#
add R82
del R89

Avoid leakage issue

PIN44 / PIN7 / PIN5

LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

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Mini PCI-E Card 2- Full size MINISATA

8/23 A-->B update.

PROJECT : QLM
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	MINI PCIE CONN	1A

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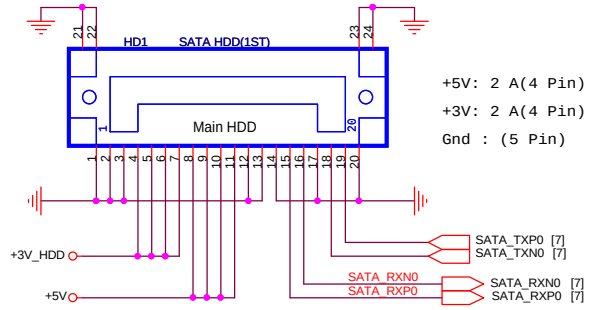
SATA HDD CONNECTOR

DFHD20MR005

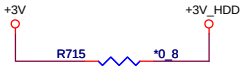
DC Current rating: 0.5 A

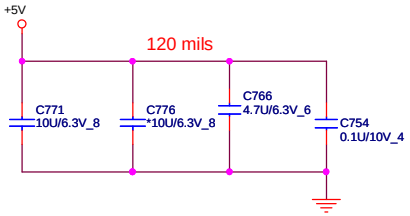


+5V: 2 A(4 Pin)

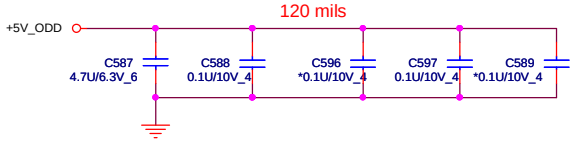
+3V: 2 A(4 Pin)

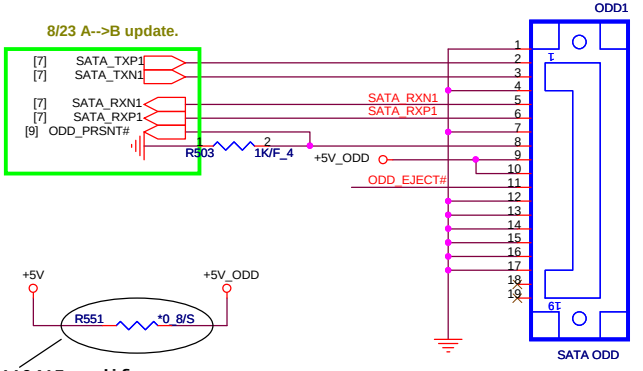
Gnd : (5 Pin)





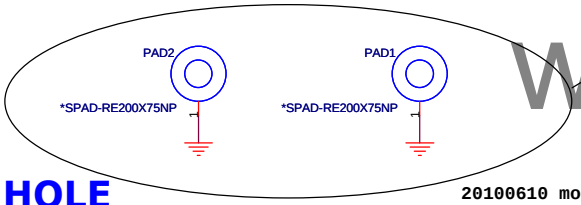
SATA CD-ROM





20110415 modify:
R551 change to short pad.

SI chenage footprint



20101122 modify:
Add PAD1 / PAD2 for EMI.

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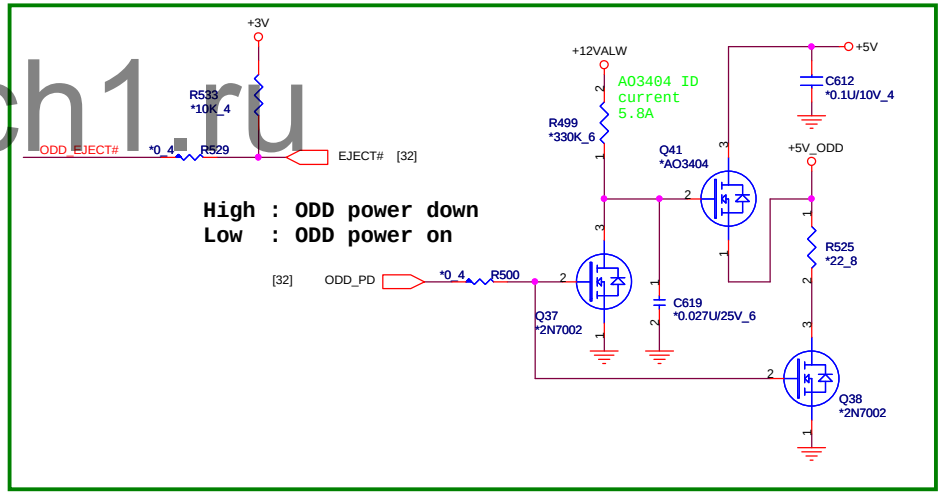
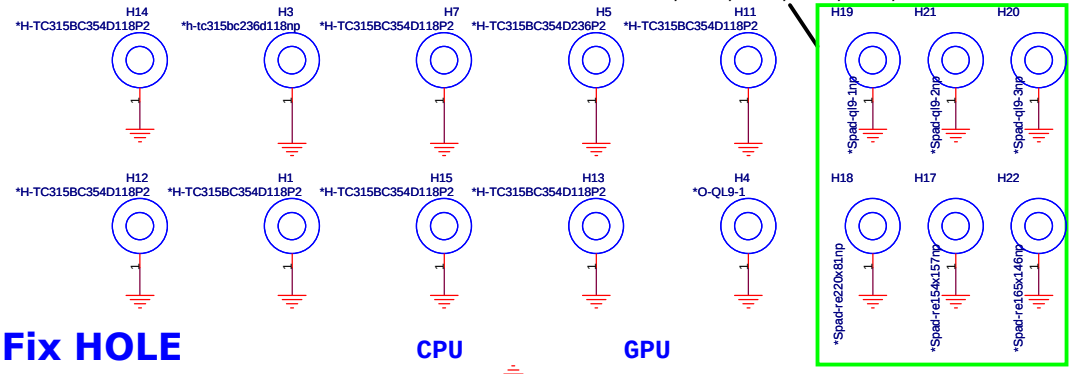


High : ODD power down

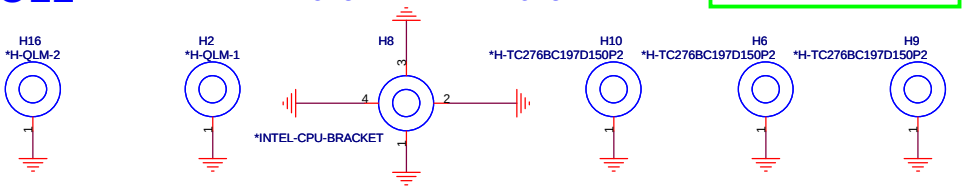
Low : ODD power on

Screw HOLE

20100610 modify:
Add H22, H23, H24, H25, H26, H27 for ME.



Fix HOLE



[22,37,41] +12VALW
[6,7,10,21,22,23,25,26,29,31,41] +5V
[2,6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,28,29,31,32,38,40,41] +3V

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/HOLES	1A

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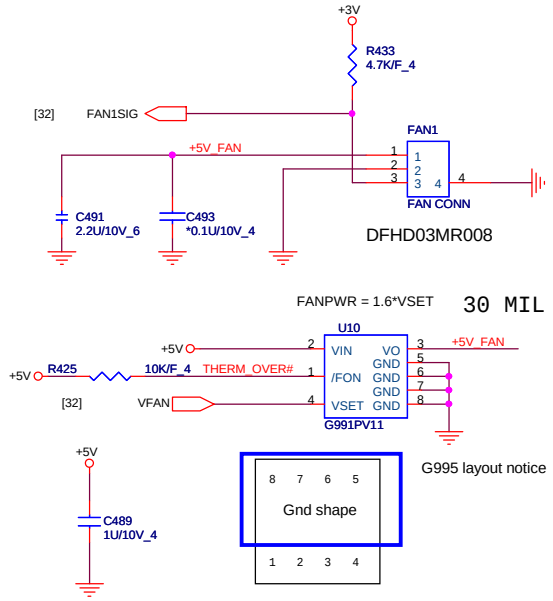
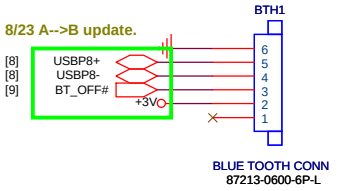
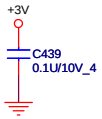
CPU FAN



BLUETOOTH

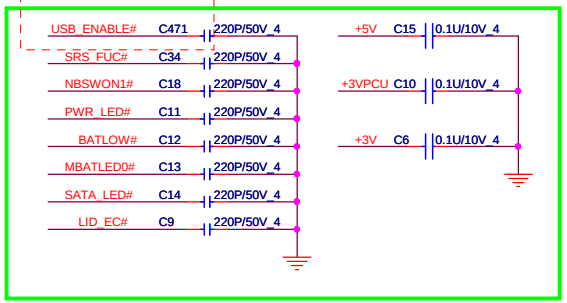


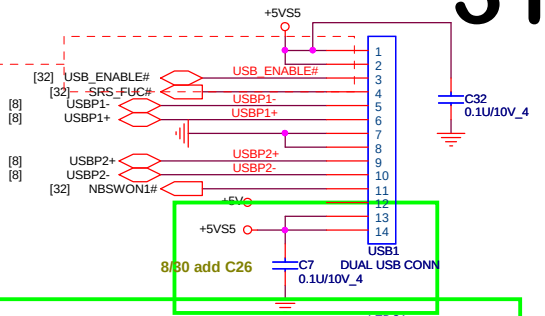


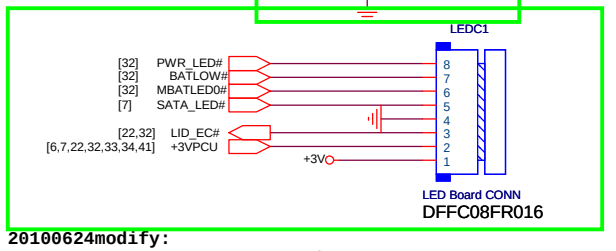
USB / LED / LID /Power&SRS Button Connector

1/27 Change netname from USB_CHR_C1 to USB_ENABLE#

20100824 modify :
for EMI request

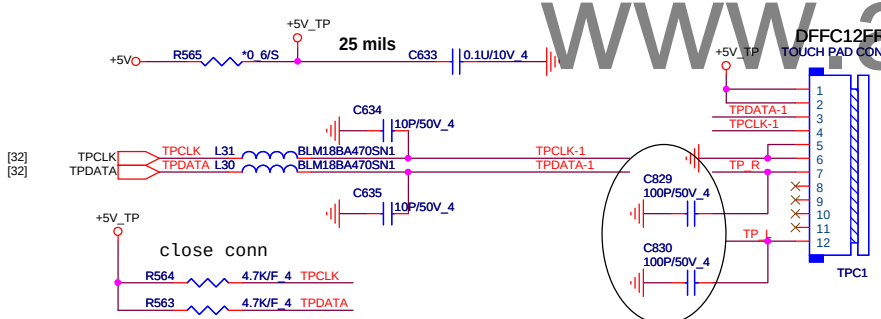




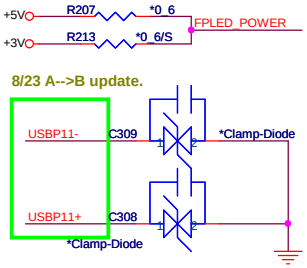


20100624modify:
LEDC1 change to pitch 1.0mm for hot bar.

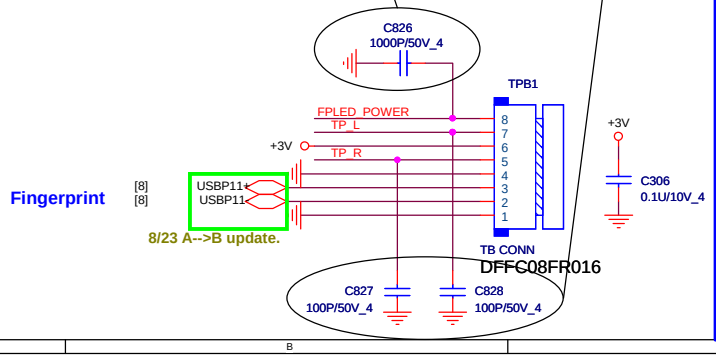
TOUCH PAD CONNECTOR



TP Button CONNECTOR

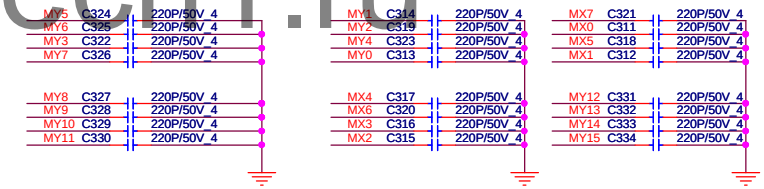


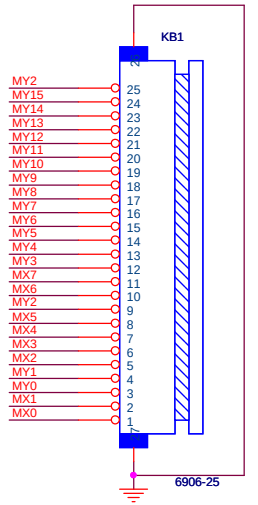
20110412 modify:
Add C826, C827, C828, C829 and C830 for EMI.



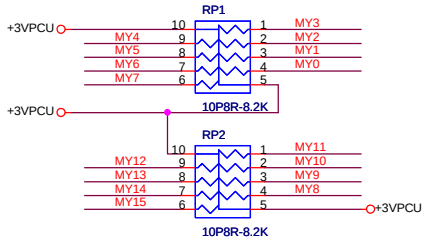
Fingerprint

KEYBOARD Con.





KEYBOARD PULL-UP



[32] MY[0..15]
[32] MX[0..7]

[10,22,28,34,35,36,37,38,39,40,41] +5VS5
[6,7,10,21,22,23,25,26,29,30,41] +5V
[2,6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,28,29,30,32,38,40,41] +3V

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USB/eSATA	1A

Date: Friday, May 20, 2011 Sheet 31 of 42

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IT8518/CX

IT8518E/DX

20110412 modify:
EC pin 85 change from HDMI_HPD to Charger_ON.

20110418 modify:
R630, R589, R641, R587 change to short pad.

20110415 modify:
R129 change to short pad.

20110412 modify:
EC pin 48 change from S5_ON to 3VS5_ON.

20110415 modify:
R177 change to short pad.

Fix LED issue

Layout Note:
Place all capacitors close to IT8502N.

12 MILS

Select Pin

	QLH Select
QLH	Ra
NC	Rb

thermal shutdown circuit

SPI FLASH MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031

1/17 Change netname DGPU_PWR_EN to USB_CHR_C3

D5 need to close PCH.

For Battery charge/charge and cap board

For PCH SMB/DDR Thermal IC/VGA

8/23 A-->B update. For SG/DIS

8/23 A-->B update.

Mount for Optimus

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PROJECT : QLM
Quanta Computer Inc.

NB5

Size: Custom | Document Number: IT8515/CX/FLASH | Rev: 1A
Date: Friday, May 20, 2011 | Sheet 32 of 42

TOP DC_JACK
65/90/120W

QLM:SI EOD

Place this ZVS close to idea diode

Do Not add test point on BATDIS_G signal

A modify footprint for EE request 0608

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to IC

Place this cap close to EC

PU2
OZ8681

PV

QLM:PV

SI:EC

Parallel

PV:EMI

SI:Acoustic

PV:ACIN circuit change for VIN drop when ITE EC reset

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PROJECT : QLM
Quanta Computer Inc.

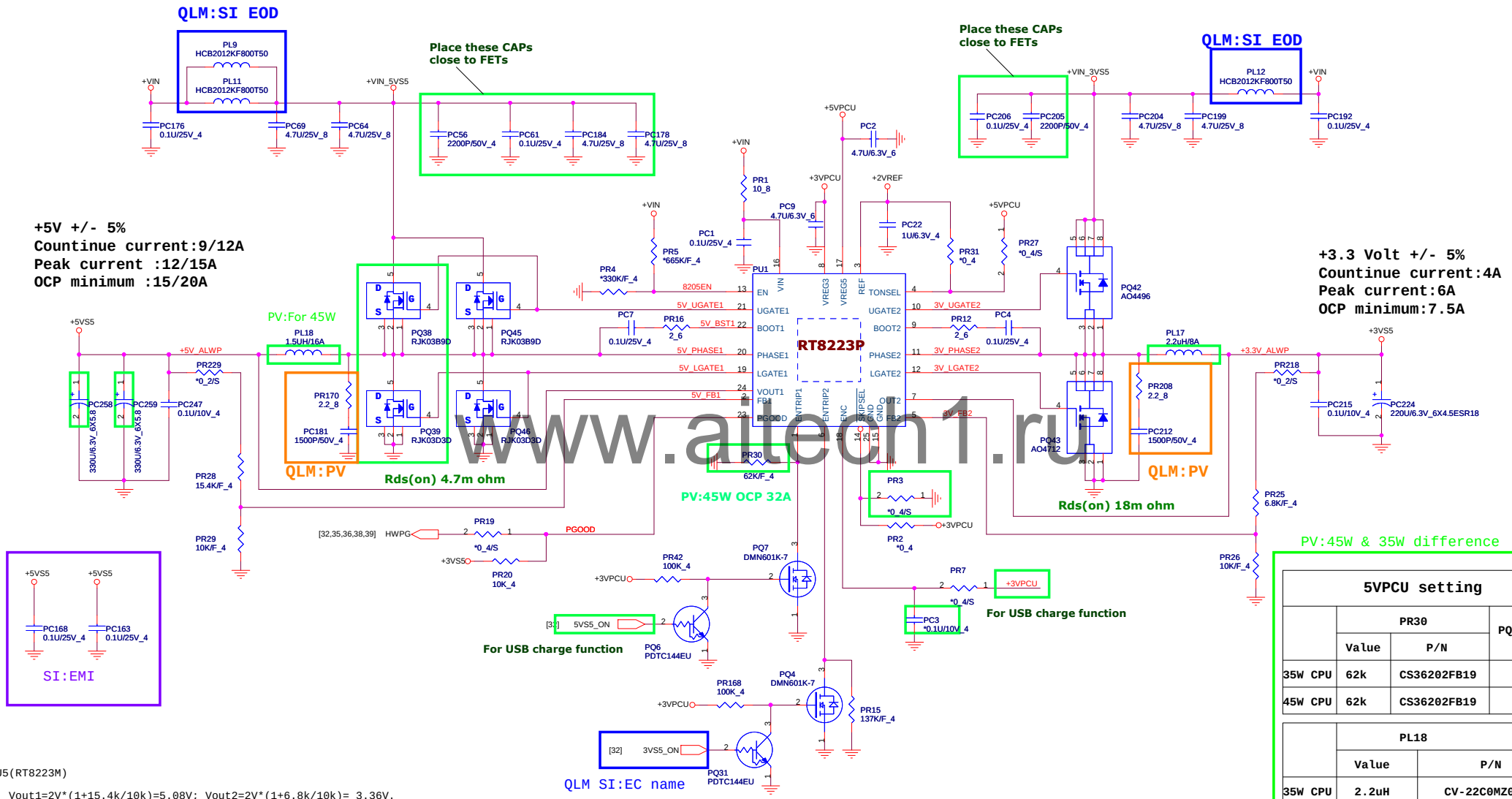
NB5

Charger (BQ24704)

Size Custom | Rev 1A

Date: Friday, May 20, 2011 | Sheet 33 of 42

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PV:45W & 35W difference

5VPCU setting			
	PR30		PQ38/PQ39
	Value	P/N	
35W CPU	62k	CS36202FB19	No POP
45W CPU	62k	CS36202FB19	POP

	PL18	
	Value	P/N
35W CPU	2.2uH	CV-22C0MZ02
45W CPU	1.5uH	CV-15G0MZ03

PU5(RT8223M)

1. Vout1=2V*(1+15.4k/10k)=5.08V; Vout2=2V*(1+6.8k/10k)= 3.36V.
2. 5V current limit = (35.7K*10uA/10/(4.7mohm/2)) = 15.1A,new version sample Entrip pin can low than 0.8V
3. 3.3V current limit = (137K*10uA/10/18mohm))=7.6A
4. Tonsel(pin4)=5V, F=400KHz/500KHz.

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NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

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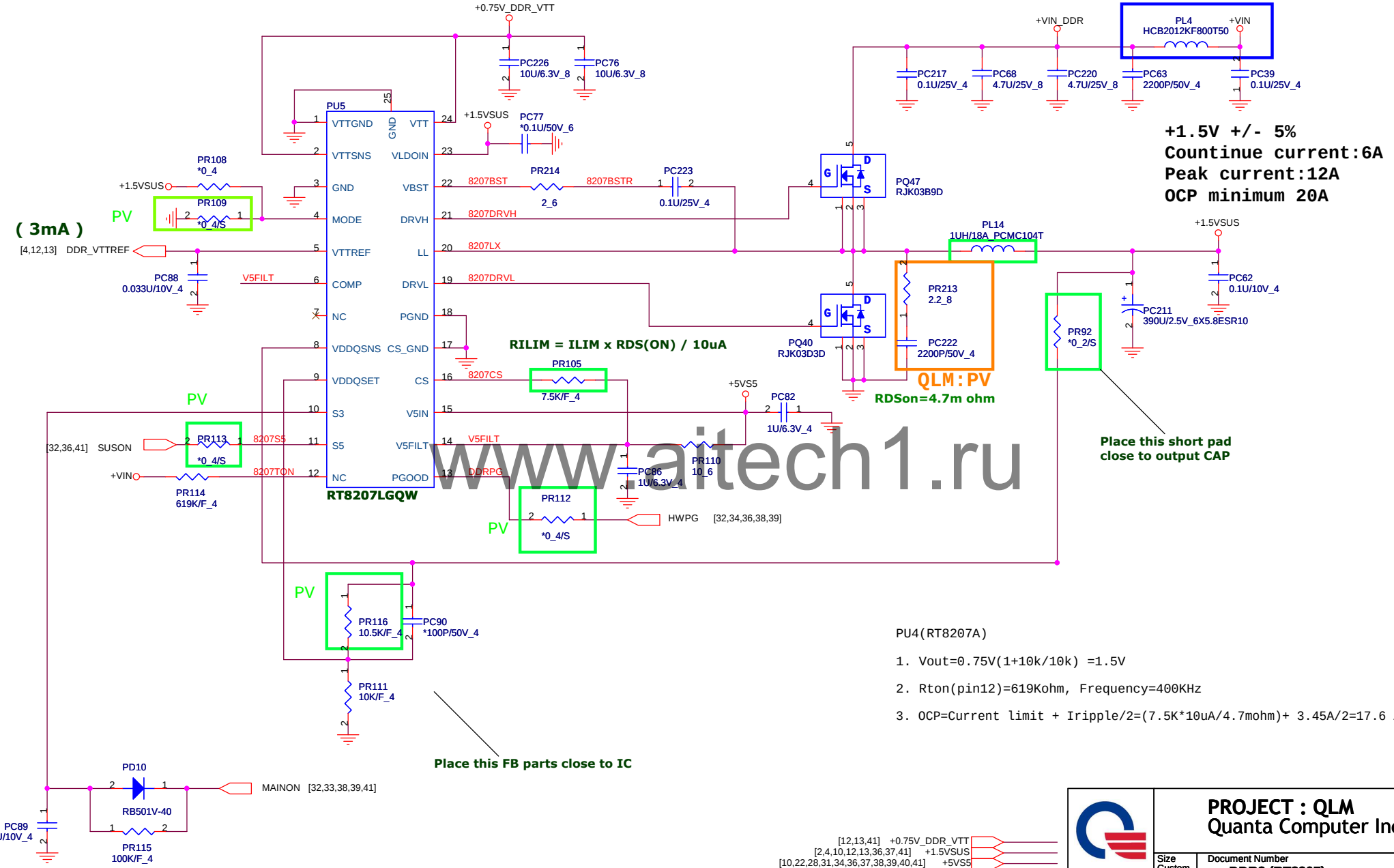
(VTT/2A)

QLM:SI EOD



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 20A

PU4(RT8207A)

1. Vout=0.75V(1+10k/10k) =1.5V
2. Rton(pin12)=619Kohm, Frequency=400KHz
3. OCP=Current limit + Iripple/2=(7.5K*10uA/4.7mohm)+ 3.45A/2=17.6 A

[12,13,41] +0.75V_DDR_VTT
[2,4,10,12,13,36,37,41] +1.5VSUS
[10,22,28,31,34,36,37,38,39,40,41] +5VS5
[22,33,34,36,37,38,39,41] +VIN

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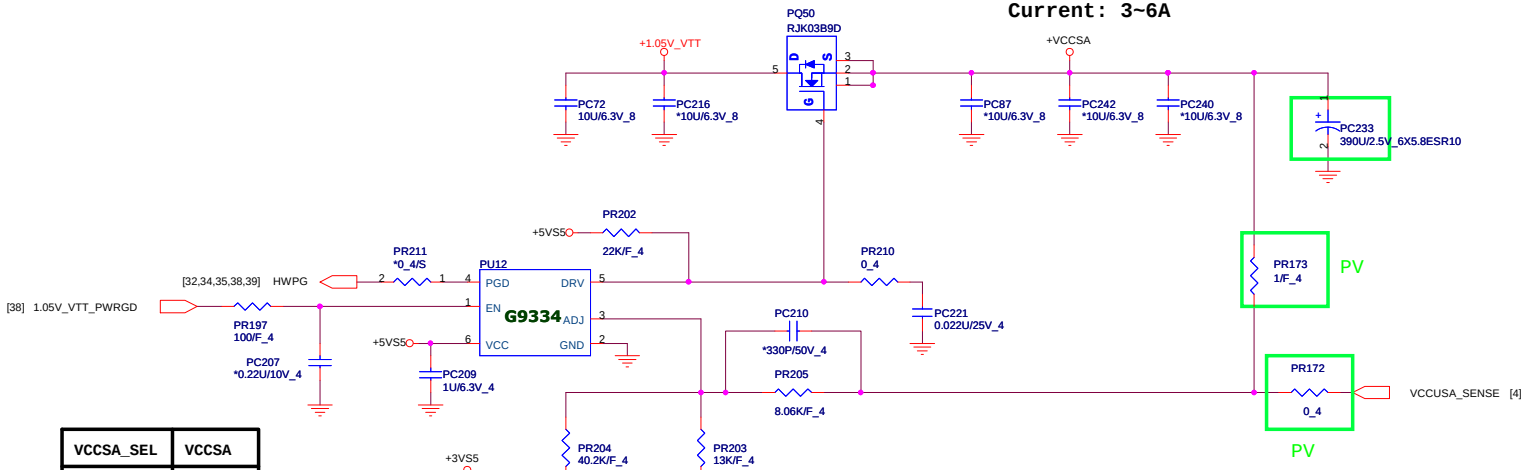
NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A
Date: Friday, May 20, 2011	Sheet 35 of 42	

VCCSA 0.8V+/- 5%
Current: 3~6A



VCCSA_SEL	VCCSA
0	0.9V
1	0.8V

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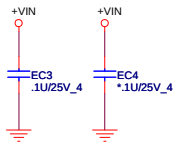
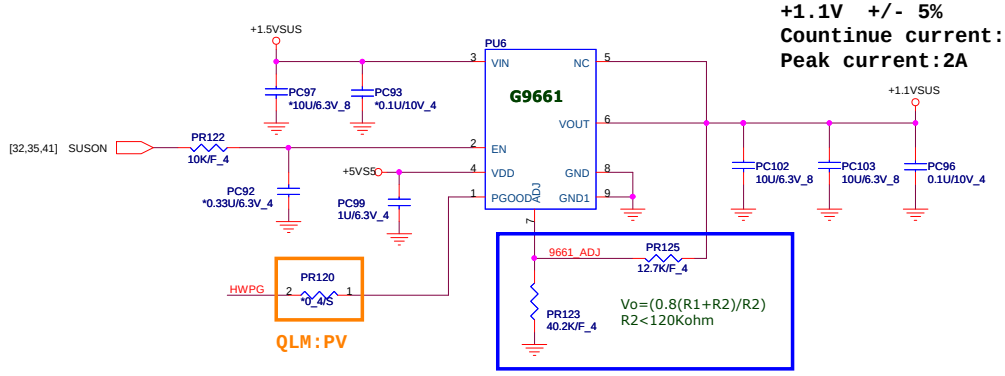


+1.1V +/- 5%
Countinue current:650mA
Peak current:2A



QLM:PV

QLM:SI change 1.1V to 1.05V

NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V_VTT (VT358)	1A

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Location	N12E-GE2
PR276	140K ohm (CS41402FB14)
PR280	48.7K ohm (CS34872FB17)
PR278	665K ohm (CS46652FB10)
PR279	137K ohm (CS41372FB12)

CNTRL1 GPIO6	CNTRL0 GPIO5	N12E-GE2
1	1	0.8125V
1	0	0.85V
0	1	NA
0	0	NA

QLM:SI EOD

+VGA_CORE +/- 5%
Countinue current:44A
Peak current:54A
OCP minimum 54A

QLM SI:change VGA to 2 phase

QLM:PV

Connect to PIN18 directly

Connect to PIN9 directly

PU17 OZ8122

Location	Optimus	Discrete
PR298	22 ohm (CS02204JA18)	NA
PQ71	DMN601K-7 (BAM601K0003)	NA
PR299	22 ohm (CS02204JA18)	NA
PQ72	DMN601K-7 (BAM601K0003)	NA
PR288	NA	20 K ohm (CS32002FB29)
PD21	NA	BAS316 (BC000316Z00)

+1.8V +/- 5%
Countinue current: 1.0A
Peak current:3A

PU18 *G9661

For Optimus NA

VO=(0.8(R1+R2)/R2)
R2<120Kohm

Reserve for new N-11 power up sequence

(5A)

(2A)

(10A)

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PROJECT : QLM
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	VGA CORE(OZ8122)	1A

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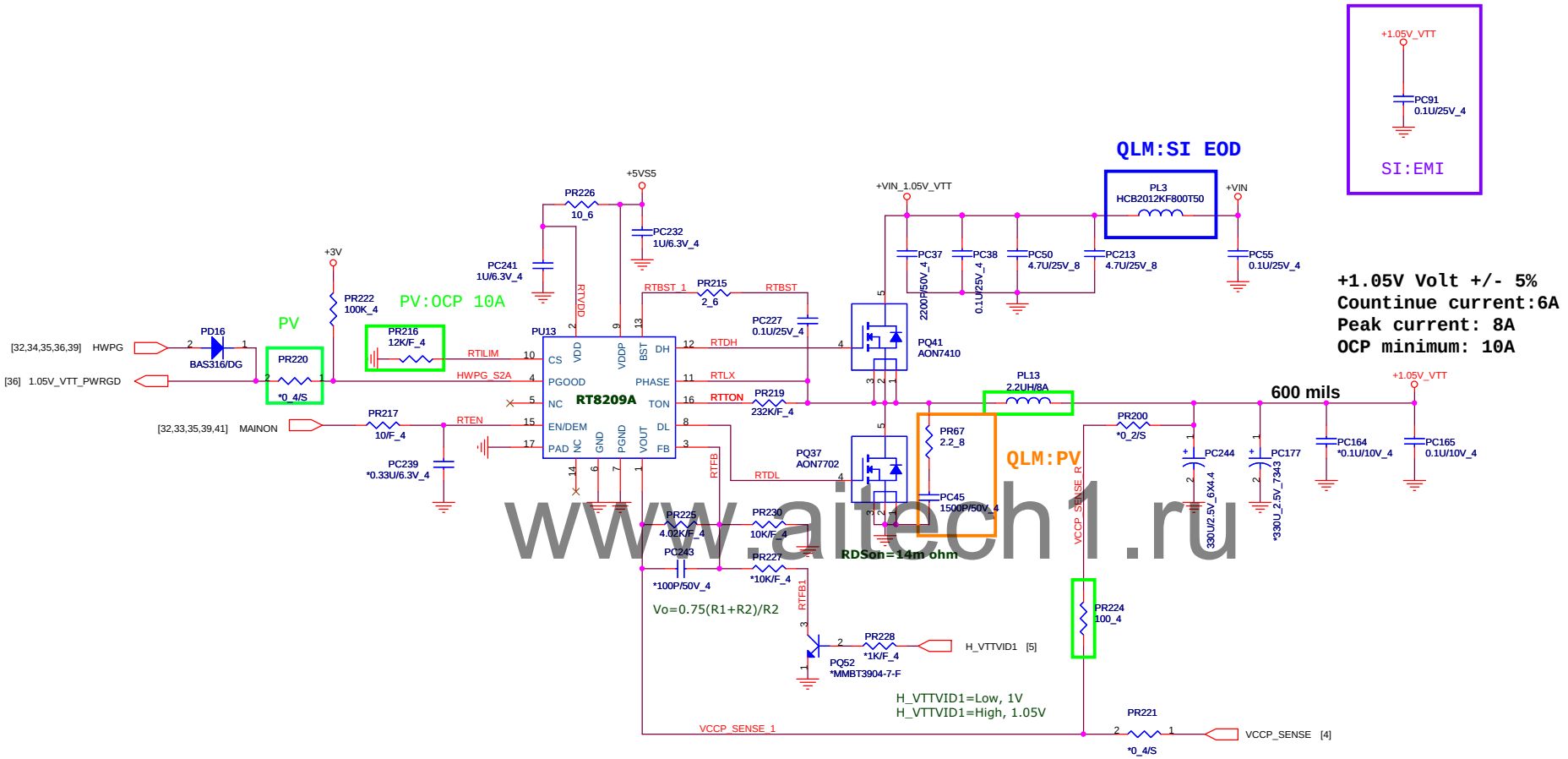

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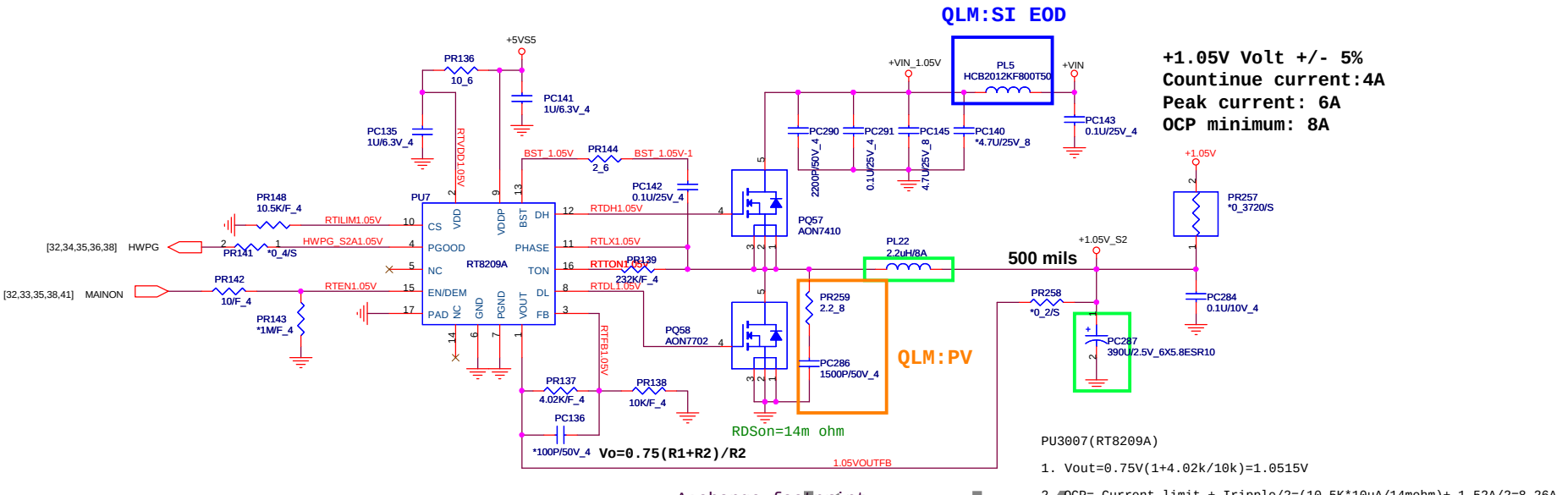
PU3006(RT8209A)

1. Vout=0.75V(1+4.02k/10k)=1.0515V
2. OCP= Current limit + Iripple/2=(14K*10uA/14mohm)+ 1.52A/2=10.76A, if OCP=20A please change PR3044 from 14k to 27k
3. RTon= 232Kohm, F=300KHz

NB5	PROJECT : QLM Quanta Computer Inc.	
Size	Document Number +1.05V_VTT	Rev 1A
Date: Friday, May 20, 2011	Sheet 38 of 42	



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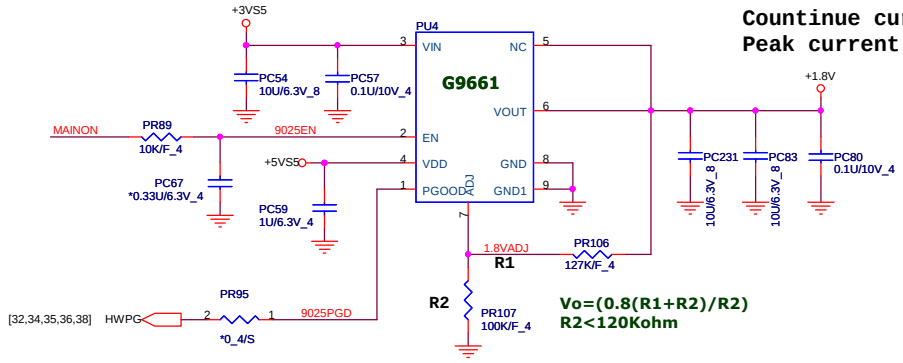
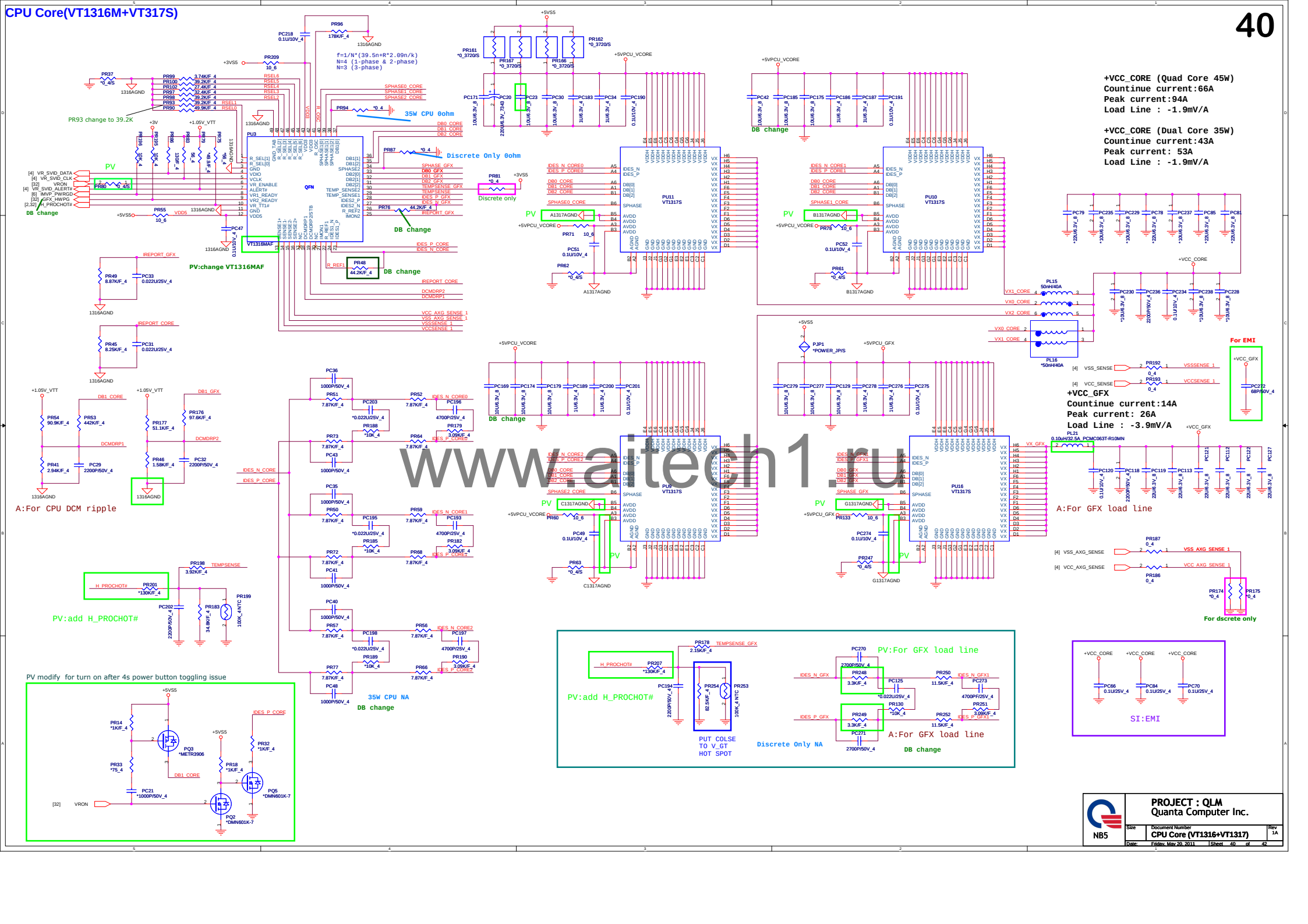


PU3005(RT9025)

1. Vout= 0.8V(1+127k/100k) = 1.816V

2. PD = 1.2A * (3.3V- 1.8V)=1.8W, RT9025 PD maximum is 1,33W

NB5	PROJECT : QLM Quanta Computer Inc.		
	Size	Document Number +1.05V / +1.8V	Rev 1A
	Date: Friday, May 20, 2011	Sheet 39 of 42	



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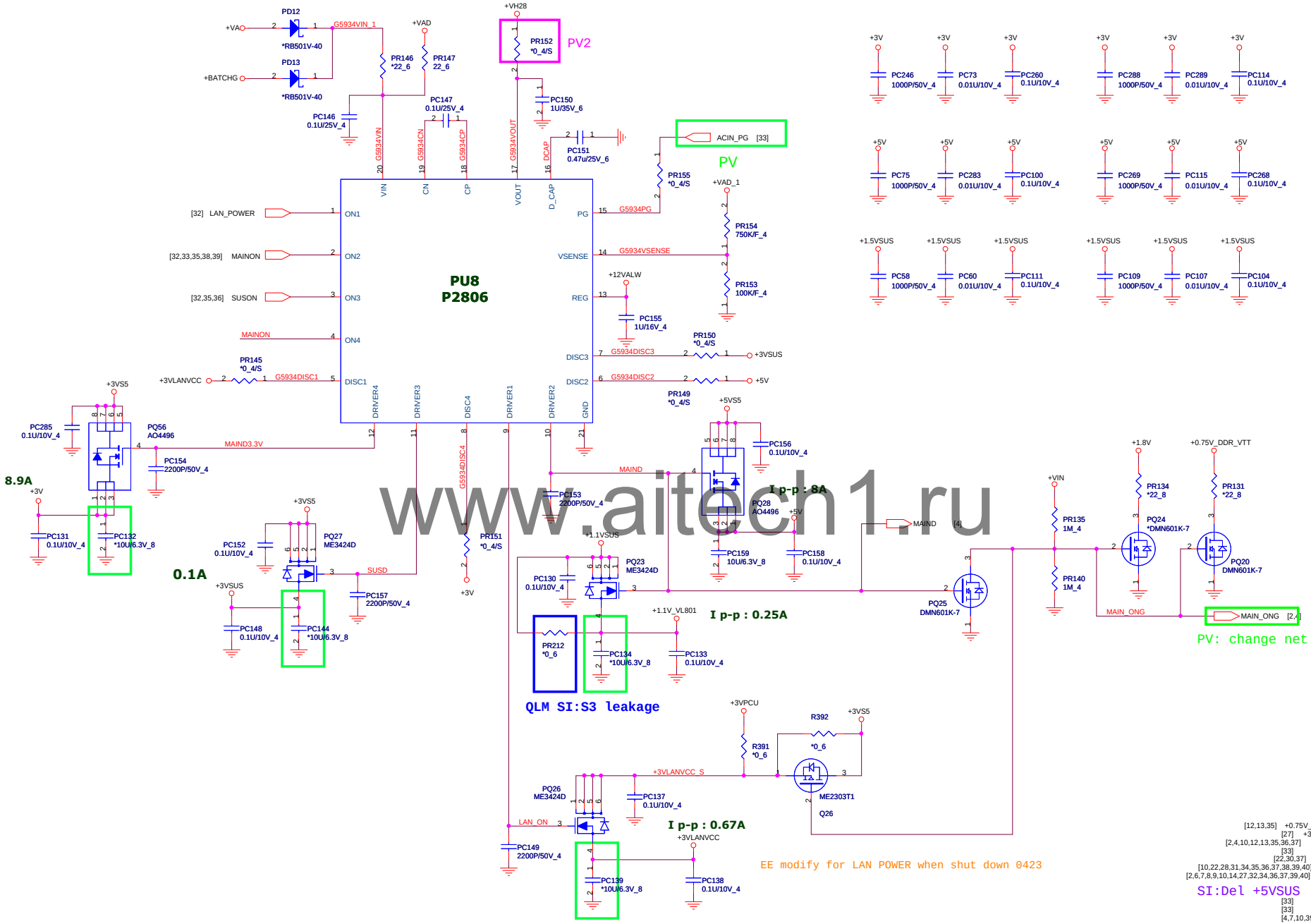
NB5	PROJECT : QLM Quanta Computer Inc.	
Size	Document Number CPU Core (VT1316+VT1317)	Rev 1A
Date: Friday, May 20, 2011	Sheet 40 of 42	



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NB5	PROJECT : QLM Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (P2806)	Rev: 1A
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QLM Pre-A to DV1 modify history

Page 02: 1. Mount C417, C418, C410, C411, RP5.

Page 12: 1. Add R817, R818, R819, R820, R821, R822, R823, R824, R825 for EMI.

Page 31: 1. Modify TPC1 pin define for new TP module.

QLM DV1 to DV2 modify history

Page 02: 1. R428 Change to 25.5 ohm for intel DG.
2. RP4 change to unstuff for no ePD.
3. CLK_DPLL_SSCLKP_R change to pull down 1K.
4. CLK_DPLL_SSCLKN_R change to pull up 1K.

Page 06: 1. R293 change to short pad.

Page 07: 1. R669 change from 10K to 1K for S3 issue.
2. Add C240 for S3 issue.
3. R337 change short pad.

Page 08: 1. Delete R362, R378, R375, R353, RP5.

Page 09: 1. R614 change to short pad.

Page 10: 1. DV2 add +5V_S5 leakage issue.
2. R330, R335, R663 change to short pad.

Page 14: 1. Delete R173 and add NET: VSS_GPU_SENSE.
2. R126 change to short pad.
3. L27 change to short pad.
4. Delete pin D35, P7, E35, R7 contact net.

Page 18: 1. Delete C240, C209.
2. Add C831 330uF for reduce +VGACORE ripple noise.

Page 22: 1. R399 change to short pad.

Page 24: 1. CN2 modify 4 pin GND CONN for EMI.

Page 28: 1. Add NET Charger_ON and R774 to U16 Pin5.
2. R762 change from 4.7K to 1K for S3 issue.
3. Add C209 for S3 issue.
4. CN5 change footprint for SMT issue.
5. Add D32 for USB 3.0 ESD.
6. Stuff C647 and C646 for USB 2.0 ESD.
7. R769 change to short pad.
8. R711 change to short pad.
9. Reserve R775.

Page 30: 1. R551 change to short pad.

Page 31: 1. Add C826, C827, C828, C829 and C830 for EMI.

Page 32: 1. EC pin 85 change from HDMI_HPD to Charge_ON.
2. EC pin 48 change from S5_ON to 3VS5_ON.
3. R129 change to short pad.
4. R177 change to short pad.
5. R630, R589, R641, R587 change to short pad.

QLM DV2 to PV modify history

Page 21: 1. Q39, Q40 change from FDV301N to 2N7002.

Page 22: 1. C26 and C27 change from reserve to 10pF for EMI.

Page 24: 1. R385 change from 33 to 0 ohm for EMI.
2. R386 change from 0 to 33 ohm for EMI.
3. C446 change from reserve to 10pF for EMI.

Page 28: 1. Add R335, R776, R353 for reserve TPS2543.
2. Add RP7 for EMI.

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NB5

PROJECT : QLM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	History	1A

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